Video Rate JPEG KL5A71007 datasheet

revision 1.4

revision history

rev 0.1	97.1.27	First Draft
rev 0.2	97.3.13	Register re-defined. 80pin pitch changed.
rev 0.2 a	97.6.25	AC-timing added
rev 0.3	97.9.22	
rev 1.0	98.4.24	Characteristics fixed
rev 1.1	98.9.10	IDDS re-defined
rev 1.2	99.1.19	add max data reg
rev 1.3	99.7.22	add DHT notice
rev 1.4	99.12.2	FBGA80 canceled

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0)Contents

Chapter

1)Introduction -- Product feature

KL5A71007 LSI is Kawasaki LSI's one chip JPEG hardware solution, which is enhanced its performance while maintaining the ease-of-use chip interface its precedence KL5A71006A has. This new chip has 8 times faster in operation than the previous chip.

KL5A71007 can process either JPEG baseline compression or decompression by user setting. Although chip throughput deeply depends on the system configuration, Kawasaki set the chip design goal as follows.

- Optimized peak image processing throughput is 32Mbytes/sec.

For YUV 4:2:2 sampling color space data, VGA size (640 pixel by 480 line) one frame data is compressed or decompressed in around 20.5 milli-second by KL5A71007. For SXGA image (1,280 pixel by 1,024 line), this chip can produce to or reproduced by the compressed data in around 83 ms.

Both quantization table (Q-Table) and Huffman table (H-Table) are stored in on-chip RAMs. User can easily build up the table with writing table data, whose data entry sequence is very similar to that of JPEG DQT and DHT marker format.

KL5A71007 can produce to or re-produce image from the compressed data, which complies ISO/IEC 10918-1 JPEG standard baseline process.

In addition to produce the bit stream data, KL5A71007 can handle JPEG header information, RST marker generation/decode by itself.

KL5A71007 has several data transfer modes, which expands the flexibility of system configuration.

--------- calculus example ----------
For VGA processing time

VGA image data volume = (640 x 480)pixel/frame x 2bytes/pixel
= 614.4 kbytes /frame

Suppose the chip's peak throughput is 32Mbytes/sec
total time to compress or decompress = 614.4 k /(32M) sec
= 19.2 ms/frame

By adding 1.3ms due to initialization and some overhead,
we will get 20.5 ms for VGA size YUV 4:2:2 one frame processing.

Based on the same consideration, we can get 81.92 ms for 2,621.44 kbyte data. With 1.1ms margin, the chip will take 83ms to process SVGA size YUV 4:2:2 one frame data.

For pixel data transfer, user can select one of the following mode.
- PCLK synchronous mode (thru pixel bus)
- pixel DMA dedicated mode (thru pixel bus)
- pixel DMA timesharing mode (thru host bus)
- register access mode (thru host bus)

For code data transfer, either mode can be selected.
- host DMA mode (thru host bus)
- register access mode (thru host bus)

When choosing PCLK synch mode or pixel DMA dedicated mode, pixel data can be transferred in parallel with code data transfer. Both transfer uses the separated bus and user can make full use of the system hardware resources.

When using pixel DMA timesharing mode or register access mode, user accesses both pixel and code data through host bus.

User can select bus size (16bit or 8bit), endian (big or little) of pixel bus and host bus separately by setting the internal register bits.

Please note that pixel data is assumed to be transferred in block interleaved format. Number of components and relative sampling ratio are user selectable within JPEG baseline specification.

To reduce the power consumption in idle mode, user can stop the chip internal clock by asserting the external LOWPWR pin. Chip goes into low power mode.

Chip is molded into the thin flat package LQFP with 0.5mm lead pitch. There are two types of LQFP package depending on user application.
For full use of KL5A71007 JPEG function, LQFP-80 (80pin, 12mm-sq mold size) is the best choice. Another selection is LQFP-64, which is smaller (10mm-sq mold size).
For LQFP-64, the PLL function is not available and the width of pixel bus is restricted to 8 bits to save the pin count.

2) Specification overview

KL5A71007 is designed under the following specification.

a) compress/decompress method

- compliant with the JPEG standard baseline process[4] (ISO/IEC 10918-1)

b) digital imaging data format

- each component has 8 bit data.
- endian selectable
- block interleaved format[5]
- unsigned or binary offset to be converted 2's compliment
- data is level shifted (-128) internally

c) chip throughput

- max 32M bytes/sec at internal clock rate 32MHz

d) marker code to be processed

- for compression

SOI, DHT, DQT, DRI, SOF0, SOS, RSTm, EOI markers are generated and attached as header information.

- for decompression

SOI, DHT, DQT, DRI, SOF0, SOS, RSTm, EOI, DNL markers are decoded and used for data processing.

APPn followed by Lp bytes and COM followed by Lc bytes are completely ignored by the chip.

e) quantization table

- 4 sets of programmable table area (RAM, up to 4 components)

f) Huffman table

- 4 sets of programmable table area (RAM, 2 for DC table and 2 for AC table)

g) table setting

- programmed by CPU through host interface or by reading the header data.
- header data can be used during compression
- data without table information can be decompressed by using pre-setting table data

h) input/output bus

- pixel bus
  Used at PCLK synchronous mode and pixel DMA dedicated mode.
  Bus width is 8bits for LQFP-64 and 8bits/16bits selectable for LQFP-80.

- host bus
  Used for code data transfer at register access mode or host DMA mode.
  Also used for pixel data transfer at register access mode or pixel DMA timesharing mode.

i) input/output buffer

- LVTTL compatible buffer.

j) power voltage

- 3.3 volt +/- 0.3 volt

l) clock rate

- internal clock rate max 32 MHz
- external clock rate max 32 MHz (PLL no use) max 16 MHz (PLL use)

m) low power mode

- stop the internal clock

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4) JPEG baseline process
The basic feature of the JPEG baseline process is summarized as follows. (extracted from CCITT Rec. T.81 p.22)

- DCT-base process
- image data

8bits per component. Unsigned or binary offset.
Input data is level shifted (-128) internally.

- sequential coding (All components are coded into one scan)
- Huffman coding

2AC and 2DC tables

- Decoder

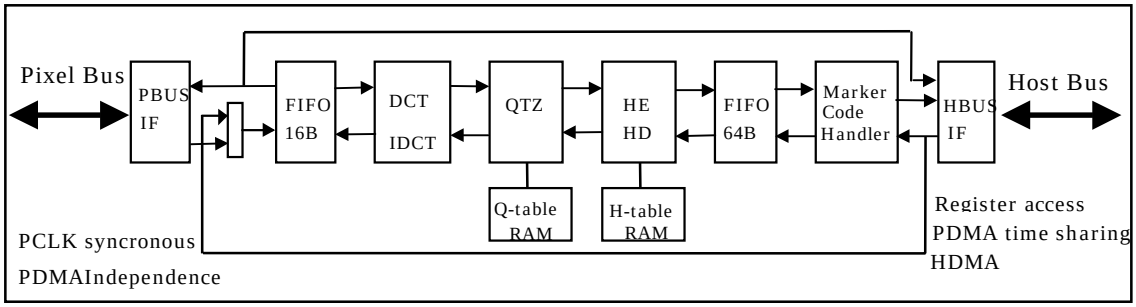
up to 4 components can be processed

- interleaved (Ns > 1) and non-interleaved (Ns = 1) scan

5) block interleaved format
Input data is grouped by component constructing block data which is corresponding to 8 by 8 pixel data. Then block data is interleaved. Each data in the block is sequentially transferred (from upper left to lower right).

3) Chip interface and reset operation

internal block diagram



Functional block diagram

chip function overview

Data processing flow is as follows.

In compress operation, pixel data in block interleaved format is fed in 16Byte FIFO through PBUS interface from pixel bus or through HBUS IF from host bus. Pixel data is converted to DCT coefficients by DCT/IDCT block. DCT coefficients are quantized by QTZ block, which use the quantize coefficient stored in Q-table RAM. Quantized DCT coefficients are converted to Huffman code by HE/HD block. Huffman code data is sent to 64Byte FIFO. With JPEG formatting (Marker attached), code data is out to the host bus
through HBUS IF.

In decompress operation, JPEG code data is sent to 64Byte FIFO via Marker Code Handler, where marker code is decoded and stripped. code data is Huffman decoded, de-quantized and inversely transformed to the pixel data. Pixel data is sent to 16Byte FIFO and out to the pixel bus through PBUS IF or to the host bus through HBUS IF.

Both Quantization coefficients and Huffman codec information are stored in RAM, where values are programmable and are set at the beginning of the operation by loading outside or extracting from the incoming JPEG data.

detail data transfer mode explanation

There are several mode to transfer the pixel and code data to/from outside. Four modes are presented for the pixel data transfer (a to d). Two modes (e and f) are shown for the code data transfer.

a) PCLK synchronous mode (thru pixel bus) - pixel transfer

With external PCLK, the pixel data is sent or received from the JPEG chip through pixel bus. Bus width can be changed 8bit (default) to 16bit by setting the internal register value. For 8bit operation, PCLK is used as the internal clock. For 16bit operation, internal PLL generates double frequency of PCLK, which is used as internal clock and the pixel data can be accessed continuously. Incoming or outgoing pixel data can be holded by VALID and HOLD handshake. Pixel data sender can stop sending data by negating VALID. Pixel data receiver can hold the incoming data by asserting HOLD signal. Both operation can be performed independently each other. Direction of pixel bus is determined by the flags in mode register (HADDR = h06). After the hardreset, pixel bus is set to the input direction.

b) pixel DMA dedicated mode (thru pixel bus) - pixel transfer

Pixel bus can also be used as DMA bus. As slave DMA device, pixel data can be transferred with PREQ and PACK handshake.

DMA transfer is an asynchronous, which means no need to synchronize both pixel data and PACK signal with external chip clock. Both bus width and endian format can be selected by setting the bus format register (HADDR = h00). Internal clock is also selectable by using PLL as external clock doubler or by using the external clock itself.

c) pixel DMA timesharing mode (thru host bus) - pixel transfer

Instead of using pixel bus, host bus can be used in pixel data DMA transfer. This is one of the host bus timesharing operation. Pixel data is transferred to the 16bit FIFO automatically in the chip. Pixel data DMA transfer through host bus is performed by PREQ and PACK handshake. User also can use HRDN and HWRN control signals in cope with PACK by selecting the flag of mode register (HADDR = h06). Bus width, it's endian format and internal clock generation method are the same as the description in b).

d) register access mode (thru host bus) - pixel transfer

Pixel data can be transferred by using the register access mode through host bus in timesharing operation. External controller drives the pixel data register address (HADDR = h2E), asserts the control signal - HRDN or HWRN and transfers the pixel data. Transaction is not ended until asserting the HRDY signal by JPEG chip.
This HRDN/HWRN - HRDY handshake is exactly the same as that of JPEG

chip internal register access. To assure the correct operation, HRDY assertion is always verified by the external controller before the termination of transaction each time. It is strongly recommended that the external controller checks the status register (HADDR = h30) every time before accessing the pixel data register to see the pixel data is available or not. Otherwise the deadlock might occur because JPEG chip requires the code data to proceed the operation while the external controller is waiting for the ending of the pixel data transfer, which will never end due to the internal buffer full or empty.

e) host DMA mode (thru host bus) - code transfer

Code data can be transferred by using host DMA mode through the host bus. Handshake is HREQ and HACK. As is the pixel DMA timesharing mode, HRDN or HWRN control or just HACK control is user selectable by choosing the mode register (HADDR = h06).

DMA transfer is the asynchronous to the external clock. The host bus width and endian format are set by the flag of the corresponding internal register. For internal clock generation, please refer to the description in b).

f) register access mode (thru host bus) - code transfer

Code date also can be transferred by using the register access mode. Its register address is h2C (code data register).
Treatment of HRDY and the method to avoid the deadlock described in pixel data transfer using register access mode section are also true here. Please refer to d) for detail discussion.

soft-reset operation

In addition to be reset by the external reset pin, the chip can be reset by setting the register bit with register access.

This operation is called "soft-reset". The register address of the corresponding register flag is h24. Please note that the data in the system registers is NOT cleared by the soft-reset operation.

lowpower operation

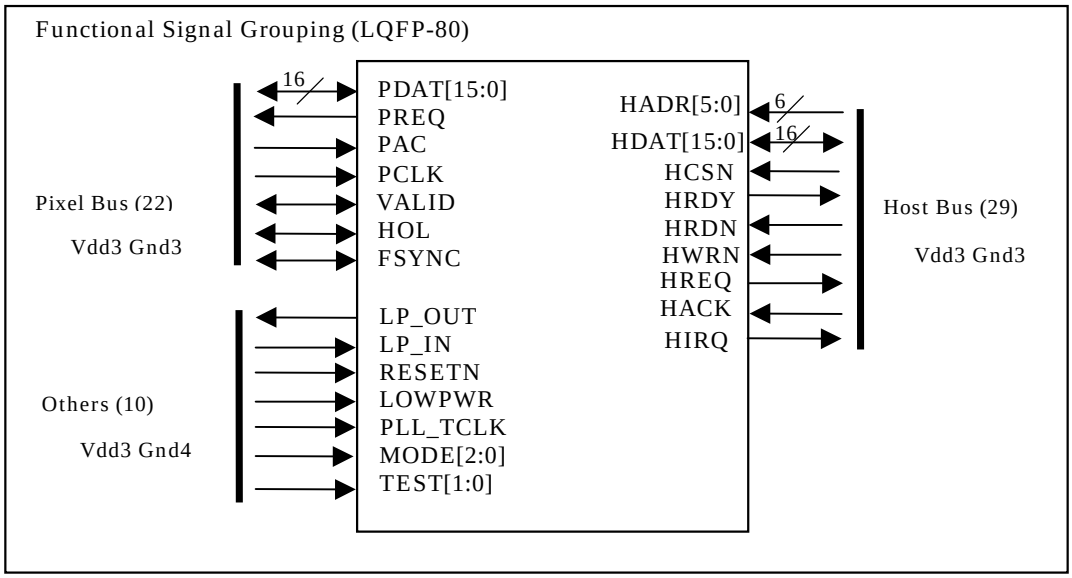
To save the power consumption when the chip is not in operation, external lowpower pin is useful. By pulling the LOWPWR pin to L, internal clock is stopped and the chip goes into the lowpower mode. It is strongly recommended to avoid lowpower setting during compress or decompress

operation. When releasing the LOWPWR pin to H, the chip is recovered from the lowpower mode. Before doing the compress or decompress operation, soft-reset operation is required.

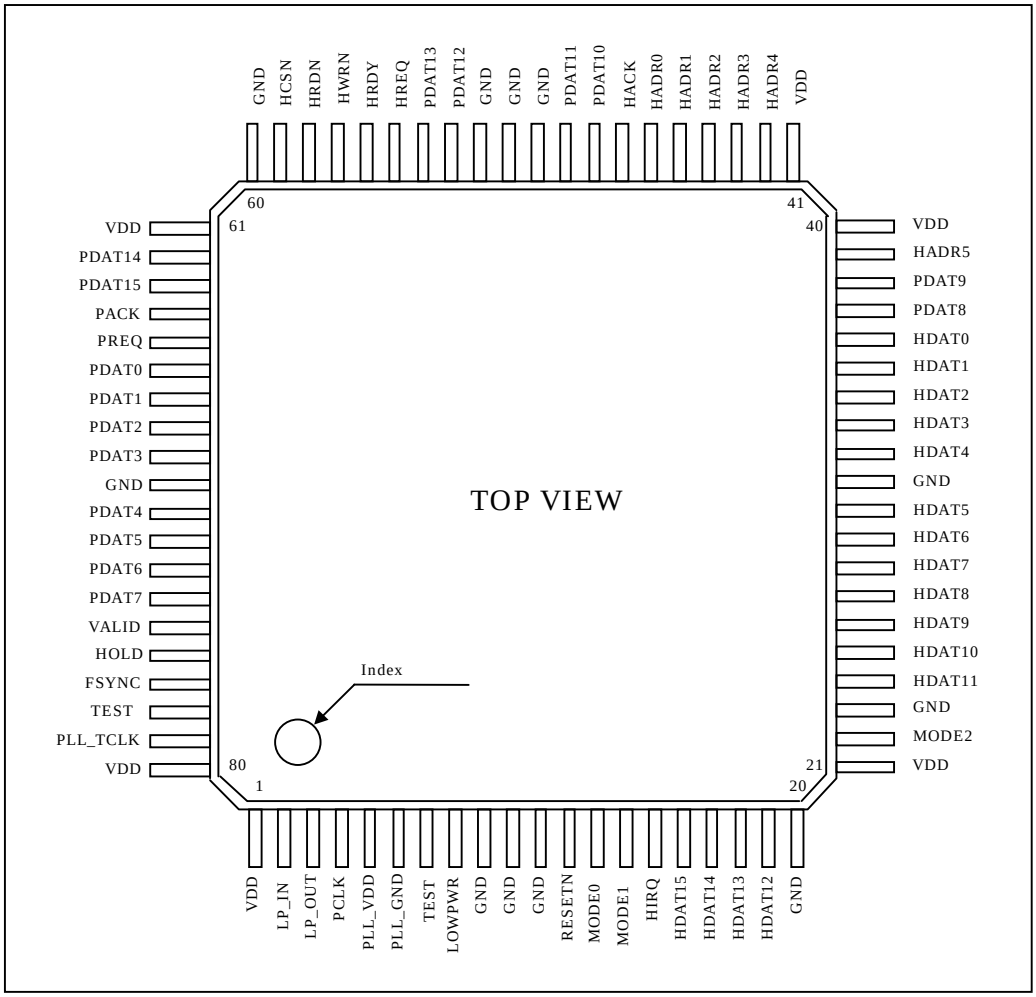
If internal PLL function is used by setting the MODE pins to an appropriate value, 2 msec lock-time is needed after the release of LOWPWR pin to guarantee the PLL lock-time. Then softreset is expected before starting the compress or decompress operation.

4) 80pin LQFP Pin Layout (LQFP-80)

4.1 Functional Signal Grouping



4.2 Pin Assignments (Top view)



5) Signal Descriptions(LQFP-80)

No.	Signal	Pin	I/O	Function
∗Host Bus				
1	HADR[5:0]	39, 42-46	I	The HADR[5:0] are "Host Bus Address" signals and provide internal register address.
2	HDAT[15:0]	16-19, 24-30, 32-36	I/O	The HDAT[15:0] are "Host Bus Data" signals and used for transferring internal register data, compressed data, and pixel data in time sharing DMA mode and register access mode. Data bus width can be selected 16 bits (word transferring) or 8 bits (byte transferring) by internal register, which is set 8 bits after hard reset. In word transfer, endian format also can be selected by internal register, which is set little endian format after hard reset. LSB is HDAT[0].
3	HCSN	59	I	The HCSN is "Host Bus Chip Select" and active low signal. When asserted, KL5A71007 recognizes as register access mode.
4	HRDY	56	OT	The HRDY is "Host Bus Ready" and active high signal. When asserted, it indicates the end of data writing or the permission of data reading. It is driven while HCSN is asserted.
5	HRDN	58	I	The HRDN is "Host Bus Read Strobe" and active low signal. When asserted, reading operation is executed. In register access mode, HDAT are read at HRDY asserted timing. In Host Bus DMA mode without HRDN and HWRN, please connect to L.
6	HWRN	57	I	The HWRN is "Host Bus Write Strobe" and active low signal. When asserted, writing operation is executed. In register access mode, HDAT are written at HRDY asserted timing. In Host Bus DMA mode without HRDN and HWRN, please connect to L.
7	HREQ	55	O	The HREQ is "Host Bus DMA Request" and active high signal after hard reset. In Host Bus DMA mode, HREQ is asserted when data transfer is permitted, and requires DMA access. The Active level can be selected by internal register.
8	HACK	47	I	The HACK is "Host Bus DMA Acknowledg-ment" and active high signal after hard reset. When asserted, KL5A71007 negates HREQ. In Host Bus DMA mode without HRDN and HWRN, transfer is executed by HACK only. The active level can be selected by internal register.

5) Signal Descriptions (LQFP-80)

No.	Signal	Pin	I/O	Function
*Host Bus				
9	HIRQ	15	O	The HIRQ is "Host Bus Interruption Request" and active high signal after hard reset. When the event occurs which is monitored by permission bits of IRQ flag register, KL5A71007 sets IRQ flag bits and asserts HIRQ. After reading the IRQ register or reset, the flag bits are cleared and HIRQ is negated. In reset, permission bits are also cleared. The active level can be selected by internal register.
*Pixel Bus				
10	PDAT[15:0]	63-62, 54-53, 49-48, 38-37, 74-71, 69-66	I/O	The PDAT[15:0] are "Pixel Data Bus" signals and used for transferring pixel data in PCLK synchronous mode and individual DMA mode. Data bus width can be selected 16 bits or 8 bits by internal register, which is set 8 bits after hard reset. In word transfer, endian format also can be selected by internal register, which is set little endian format after hard reset. In byte transfer, please connect upper byte to H or L. Or in time sharing DMA mode and register access mode, please connect PDAT to H or L. LSB is PDAT[0].
11	PCLK	4	I	The PCLK is "System Clock" signal. KL5A71007 operates according to this clock. In PCLK synchronous mode, Pixel data is processed by every PCLK. When LOWPWR is H, internal clock is stopped and KL5A71007 enters low power mode even though PCLK is given.
12	VALID	75	I/O	The VALID is "PDAT Valid" and active high signal. In PCLK Synchronous mode, It is asserted by output side of PDAT and indicates that PDAT are valid. Except for PCLK Synchronous mode, please connect to L.
13	HOLD	76	I/O	The HOLD is "PDAT Hold" and active high signal. In PCLK Synchronous mode, It is asserted by input side of PDAT and indicates that PDAT can not be received. After negated, PDAT transfer is resumed. Except for PCLK Synchronous mode, please connect to L.

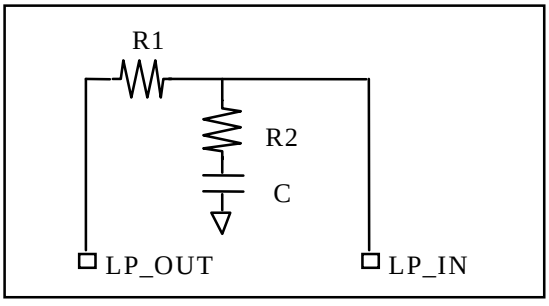
5) Signal Descriptions (LQFP-80)

No.	Signal	Pin	I/O	Function
*Pixel Bus				
14	FSYNC	77	I/O	The FSYNC is "PCLK Synchronous Transfer Period" and active high signal. In PCLK Synchronous mode, It is asserted from first data transfer to last data transfer by output side of PDAT and indicates that PDAT are transferred. Except for PCLK Synchronous mode, please connect to L.
15	PREQ	65	O	The PREQ is "Pixel Bus DMA Request" and active high signal after hard reset. In Pixel Bus DMA mode both time sharing and individual, PREQ is asserted when data transfer is permitted, and requires DMA access. The active level can be selected by internal register.
16	PACK	64	I	The PACK is "Pixel Bus DMA Acknowledg-ment" and active high signal after hard reset. When asserted, KL5A71007 negates PREQ. In Pixel Data DMA mode both time sharing and individual, DMA transfer is executed by PACK The active level can be selected by internal register.
*Others				
17	LOWPWR	8	I	The LOWPWR is "Low Power Mode Trigger" and active high signal. When LOWPWR is asserted, internal system clock is stopped and power is saved. After negated, please execute soft reset.
18	RESETN	12	I	The RESETN is "Hard Reset", and active low signal. When RESETN is asserted, all registers are cleared and KL5A71007 returns initial state, and all bi-directional pins and 3-state outputs become Hi-Z. RESETN also works same operations in low power mode. The difference between hard reset and soft reset is soft rest does not clear the registers except for Error Report.

5) Signal Descriptions (LQFP-80)

No.	Signal	Pin	I/O	Function
*Others				
19	MODE[2:0]	22, 14-13	I	The MODE[2:0] are "Chip Mode Control" signals. o b101 using PLL o b001 not using PLL If PLL is available, please input L to MODE[2] until power become stable. After that, please input H to MODE[2]. The lock time for PLL is 2ms.
20	TEST[1:0]	7,78	I	The TEST is "Test Mode Control" signal. Please connect to GND.
21	LP_IN	2	I	The LP_IN and LP_OUT are "Off-Chip Loop Filter Pin for PLL". If internal PLL is available, off-chip loop filter is needed to remove the high-frequency noise element as shown Fig. 5.1. Otherwise, please connect LP_IN to GND, and open LP_OUT.
22	LP_OUT	3	O	
23	PLL_TCLK	79	I	PLL_TCLK is "PLL Test Clock". Please connect to GND.
24	PLL_VDD	5	VDD	PLL_VDD is "PLL Power Supply". Please connect to VDD.
25	PLL_GND	6	GND	PLL_GND is "PLL Ground supply". Please connect to GND.

Low pass filter diagram



Filter constant recommendation

No.	items	value	unit
1	R1	20	kΩ
2	R2	75	kΩ
3	C	0.01	µF

Fig. 5.1 Off-chip Loop Filter diagram

6) Registers

The definitions of internal registers are indicated below. After hard reset, the registers are set up the (def) value. If there is no (def) shown, the registers are cleared to 0. In soft reset, the registers do not changed except for Error Report Register which is cleared to (def).

If the (def) value or once set up value is used, resetting is not needed. However resetting Huffman table is needed when DHT marker code is required in every compressed data.

No.	Register Name	HADR [5:0]	field bit	Function bit definition	Function bit definition
*Interface Set Up Register					
1	Bus Mode[3:0]	h00	0	Host Bus Width	1:16bit 0:8bit(def)
			1	Host Bus Endian Format	1:Big 0:Little(def)
			2	Pixel Bus Width	1:16bit 0:8bit(def)
			3	Pixel Bus Endian Format	1:Big 0:Little(def)
	Note:In LQFP-64 package, [3:2] are ignored because Pixel Bus is 8 bits. If bit [0] is 1, even and odd register are joined. In that case, Endian Format is followed by bit [1]. For Endian Format, see 7.8.				
2	Signal Active Level[4:0]	h02	0	HREQ active level	1:assert H(def) 0:assert L
			1	HACK active level	1:assert H(def) 0:assert L
			2	PREQ active level	1:assert H(def) 0:assert L
			3	PACK active level	1:assert H(def) 0:assert L
			4	HIRQ active level	1:assert H(def) 0:assert L
3	PDATuse [0]	h04	0	PDAT use	1:use 0:not use(def)
*Initial Set Up Register					
4	Mode Specify[6:0]	h06	0	Compression/ Decompression	1:Compression(def) 0:Decompression
			1	Header Informa-tion Loading	1:by Registers(def) 0:by JPEG Header
			2	Compressed Data Output Enable	1:enable(def) 0:disable
			4-3	Compressed Data Transfer Mode	0,1:Register Access(def 0) 2:DMA(with HRDN and HWRN) 3:DMA(without HRDN and HWRN)
			6-5	Pixel Data Transfer Mode	0:Register Access(def) 1:PCLKSynchronous 2,3:DMA
	Note: Pixel Data Transfer Mode / PDAT use[0] / Mode Specify[6:5] Register Access / bx / h0 PCLK Synchronous / bx / h1 Individual DMA (PDAT use) / b1 / h2 or h3 Time Sharing DMA (PDAT not use) / b0 / h2 or h3(same as Mode Specify[4:3])				

6) Registers

No.	Register Name	HADR [5:0]	field bit	Function bit definition	Function bit definition
*Initial Set Up Register					
5	Limit Of Compressed Data Volume [15:0] (k bytes)	h08	7-0	Lower Byte of Limit	unit is 1 K bytes (from 0 K bytes to 255 K bytes)
		h09	7-0	Upper Byte of Limit	unit is 256 K bytes (from 0 K bytes to 64 M bytes)
	Note:In compression, If compressed data volume reaches this limit, KL5A71007 stops outputting HDAT but continues internal operation. After hard reset, they are cleared to 0, and then KL5A71007 does not stop outputting.				
6	Compressed Data Format[3:0]	h0A	1-0	Output format	0:normal(def) 1:normal 2:only header 3:only ECS
			2	DHT Output Enable	1:enable(def) 0:disable
			3	DQT Output Enable	1:enable(def) 0:disable
*Table Set Up Register					
7	Table Data [7:0] (byte), [15:0] (word) <write only>	h10	7-0	Table data transfer by byte	H,Q table data set up by byte
			15-0	Table data transfer by word	H,Q table data set up by word
	Note:DHT or DQT marker code segment is needed for input. In word access, if number of data byte is odd, the extra byte of last word data is ignored. Endian format is followed by internal register. These registers are not used except for table data setting up by register access mode.				
*Header Information Register					
8	Restart Interval[15:0]	h12	7-0	DRI lower byte	DRI lower byte(7:0) (0:def)
		h13	7-0	DRI upper byte	DRI upper byte(15:8) (0:def)
	Note:When set up 0, DRI and RST markers are not added in compressed data.				
9	Number of Lines (SOF;Y)[15:0]	h14	7-0	Number of lines lower byte	Number of lines lower byte (7:0) (0:def)
		h15	7-0	Number of lines upper byte	Number of lines upper byte (15:8) (0:def)
10	Number of Samples Per Line (SOF;X) [15:0]	h16	7-0	Number of samples per line lower byte	Number of samples per line lower byte (7:0) (1:def)
		h17	7-0	Number of samples per line upper byte	Number of samples per line upper byte (15:8) (0:def)
11	Number of Image Components (SOF;Nf,SOS; Ns)[15:0]	h18	2-0	No. of components in Frame (Nf)	Defined in 1(def) - 4
			5-3	No. of components in Scan (Ns)	Defined in 1(def) - 4

6) Registers

No.	Register Name	HADR [5:0]	field bit	Function bit definition	Function bit definition
*Header Information Register					
12	SOF 1st Component Information [13:0]	h1A	7-0	Component identifier C1	0-255(def 0)
		h1B	1-0	Horizontal Sampling Factor H1	0:H1=4 1:H1=1(def) 2:H1=2 3:H1=3
			3-2	Vertical Sampling Factor V1	0:V1=4 1:V1=1(def) 2:V1=2 3:V1=3
			5-4	Q table selector Tq1	0-3(def 0)
13	SOF 2nd Component Information [13:0]	h1C	7-0	Component identifier C2	1-255(def 1)
		h1D	1-0	Horizontal Sampling Factor H2	0:H1=4 1:H1=1(def) 2:H1=2 3:H1=3
			3-2	Vertical Sampling Factor V2	0:V1=4 1:V1=1(def) 2:V1=2 3:V1=3
			5-4	Q table selector Tq2	0-3(def 0)
14	SOF 3rd Component Information [13:0]	h1E	7-0	Component identifier C3	2-255(def 2)
		h1F	1-0	Horizontal Sampling Factor H3	0:H1=4 1:H1=1(def) 2:H1=2 3:H1=3
			3-2	Vertical Sampling Factor V3	0:V1=4 1:V1=1(def) 2:V1=2 3:V1=3
			5-4	Q table selector Tq3	0-3(def 0)
15	SOF 4th Component Information [13:0]	h20	7-0	Component identifier C4	3-255(def 3)
		h21	1-0	Horizontal Sampling Factor H4	0:H1=4 1:H1=1(def) 2:H1=2 3:H1=3
			3-2	Vertical Sampling Factor V4	0:V1=4 1:V1=1(def) 2:V1=2 3:V1=3
			5-4	Q table selector Tq4	0-3(def 0)

6) Registers

No.	Register Name	HADR [5:0]	field bit	Function bit definition	Function bit definition
*Header Information Register					
16	SOS 1st Component Information [3:0]	h22	1-0	Scan component selector Cs1	0:Cs1=C1(def) 1:Cs1=C2 2:Cs1=C3 3:Cs1=C4
			2	DC table selector Td1	0-1(def 0)
			3	AC table selector Ta1	0-1(def 0)
	SOS 2nd Component Information [7:4]		5-4	Scan component selector Cs2	0:not allowed by JPEG spec 1:Cs2=C2(def) 2:Cs1=C3 3:Cs1=C4
			6	DC table selector Td2	0-1(def 0)
			7	AC table selector Ta2	0-1(def 0)
	SOS 3rd Component Information [3:0]	h23	1-0	Scan component selector Cs3	0-1:not allowed by JPEG spec 2:Cs3=C3(def) 3:Cs3=C4
			2	DC table selector Td3	0-1(def 0)
			3	AC table selector Ta3	0-1(def 0)
	SOS 4th Component Information [15:12]		5-4	Scan component selector Cs4	0-2:not allowed by JPEG spec 3:Cs4=C4(def)
			6	DC table selector Td4	0-1(def 0)
			7	AC table selector Ta4	0-1(def 0)
*Control and Data Register					
17	Soft Reset[0]	h24	0	Soft reset command	1:execute 0:auto clear(def)
19	Compression/ Decompression Start Command [0]	h28	0	Start command	1:execute 0:auto clear(def)
20	Compression/ Decompression End Command[0]	h2A	0	End command	1:execute 0:auto clear(def)
21	Compressed Data[7:0](byte), [15:0](word)	h2C	7-0	Compressed Data transfer by byte	compressed data by byte
			15-0	Compressed Data transfer by word	compressed data by word
22	Pixel Data [7:0](byte), [15:0](word)	h2E	7-0	Pixel Data transfer by byte	pixel data by byte
			15-0	Pixel Data transfer by word	pixel data by word
	Note:This register is effective when pixel bus transfer is register access.				

6) Registers

No.	Register Name	HADR [5:0]	field bit	Function bit definition	Function bit definition
*Report Register					
23	Status[3:0] (read only)	h30	0	Busy status	1:busy 0:idle(def)
			1	Compressed data Access	1:allowed 0:not(def)
			2	Pixel data Access	1:allowed 0:not(def)
			3	Error status	1:error(see h36) 0:normal(def)
24	IRQ Flag[7:0] (read only [3:0])	h32	0	Data output ready	1:ready 0:flag reset(def)
			1	Last data output end	1:end 0:flag reset(def)
			2	Overflow compressed data limit	1:overflow 0:flag reset(def)
			3	Error occur	1:error 0:flag reset(def)
			4	Permission for bit[0]	1:permit 0:not(def)
			5	Permission for bit[1]	1:permit 0:not(def)
			6	Permission for bit[2]	1:permit 0:not(def)
			7	Permission for bit[3]	1:permit 0:not(def)
	Note: If upper bits [7:4] are set, KL5A71007 sets [3:0] flags and asserts HIRQ when corresponding events is occurred. If [7:4] are 0, KL5A71007 does not set [3:0] flags and assert HIRQ. After hard reset, IRQ flag and HIRQ are cleared. Lower bits [3:0] are read-only. They and HIRQ are cleared after IRQ Flag register read automatically. To confirm the overflow from the limit of compressed data volume, setting bit [6] is needed.				
25	Compressed Data Volume [15:0](kbytes, read only)	h34	7-0	Compressed data volume lower byte	less than 256kB, 1kB step (The 10th-17th power of two)
		h35	7-0	Compressed data volume upper byte	Less than 64MB, 256kB step (The 18th-25th power of two)
	Compressed Data Volume [15:0](bytes, read only)	h3E	7-0	Compressed data volume lower byte	less than 256B, 1B step (The 0th-7th power of two)
		h3F	1-0	Compressed data volume upper byte	Less than 1kB, 256B step (The 8th-9th power of two)
26	Error Report[7:0] (read only)	h36	7-0	Error report (All error occurs in decompression except h1)	h0:no errors(def) h1:overflow from the limit of compressed data volume (Compression) h2:restart interval differ from DRI h4:mismatch component ID between SOS and SOF h8:number of blocks per MCU is more than 11 h10:header parameter does not match JPEG baseline standard h20:marker segment length error h40:unknown marker code h80:huffman decode error
	Note:When error is occurred, the corresponding flag is set 1. If Error report is between h2 and h80, KL5A71007 can not operate any more. In this case, initializing by hard or soft reset is needed to recover. If Error Report is not h0, Status Register [3] is set 1. This register is cleared after reading, or hard reset and soft reset.				

7) Control and data process flow

7.1 Power On

After power on, hard reset is needed. And then, please establish "Interface Set Up registers" from Host Bus by register access mode. The value of system registers is not cleared by soft reset but hard reset.

In case of using PLL, please connect MODE[2] pin to L at power on, and connect H after power become stable. Next, please execute soft reset after 2ms lock time.

7.2 How To Establish "Initial Set Up Registers"

Firstly, to establish 'Mode Specify' register (address:h06) is needed for designation of operation and transferring way. Some examples are shown below.

Pixel bus	Host bus	SR04[0]	SR06[6:3]
a) PCLK synchronous	DMA with HRDN, HWRN	b1	b6
b) Individual DMA	DMA with HRDN, HWRN	b1	hA
c) Time sharing DMA	DMA without HRDN, HWRN	b0	hF
d) register access	register access	b0	h0

To set up 'Mode Specify' register is also needed to determine compression or decompression, and data output enable in compression.
And to set up 'Compressed Data Format' register (address:h0A) is needed to determine compressed data output format, and output enable of table information.

'Limit Of Compressed Data Volume' registers (address:h09,h08) are needed to determine the limit of output data volume in compression. The unit is K byte. If data volume is over this limit, KL5A71007 stops outputting and continues internal compress operation. The right data volume is registered in 'Compressed Data Volume' register (address:h35,h34) whether the volume is over the limit or not.

7.3 How To Establish "Table Data"

For establishing table data, writing table data to 'Table Data' register (address:h10) is needed, except for establishing by compressed data with table data. DHT and DQT marker code segment is required for written data. KL5A71007 checks the table definition length. When define the Haffman table, the register address h06 and h0A must be fixed.

In compression, if table data is required in each compressed data, table data have to be set up in every flame compression.

For only table data, continuative writing mode which can transfer plural data during one HCSN asserted period, can be used.

7.4 Set up the Header information

Before compression, write the header information to the register in register access mode. The address is from h12 to h18 and h1A to h23. Compression is done with this information.

If set the value except 0 to the register h12 and h13, the restart interval maker (RST) will add to the compressed data.

In de-compression mode, header information is set to these registers.

7.5 Compression

This section describes the compression operation with setting up described in 7.2 to 7.4. This chip will start operation when set the Start Register (register h28). If change the registers after starting the operation, This chip will not operate correctly. Register information can be read during the operation, so the status or IRQ information can be checked.

After starting this chip, the header data will be output. Read the data with asserting the HACK signal after the HREQ signal is asserted in HOST-DMA mode. In register access mode, read data from the compression data register (register address = h2C) after confirming the access flag can be accessed of the compression data of the status register (register address = h30).

When the output of the header data is completed, writing the pixel data becomes possible. In the PCLK synchronous mode after confirming the HOLD signal negated, assert FSYNC and VALID, and write the pixel data. In pixel DMA mode, after confirming the PREQ signal is asserted write the pixel data with assert the PACK signal. Write the image data in the image data register (register address = h2E) for the register access mode after confirming being able to access the register by reading the status register (register address = h30).

The output of the compression data starts from the host bus after about 180-240CLK after beginning writing the pixel data. Latency changes according to whether the access mode and the pixel data are continuously written. The access method is the same as the case of the output of the header data.

In the PCLK synchronous mode negate the FSYNC signal after the final image data is input and inform the chip of the completion of the image data input. In pixel DMA mode, set the compression and the de-compression end flag (register address = h2A) after end of the data input of the previous data of the final image input, and inform the chip of the following data is the final image data. Asserting of PREQ signal is completed after the end of the input of the image data. Refer to Figure 7-5-1 for the timing of the set of the end flag.

Set compression and the de-compression end flag as well as the case of image DMA at the image register access. The compression processing ends when EOI maker is output from the host bus.

The occurrence of the error, beginning and end of compression data output and the upper bound attainment of the amount of compression can be confirmed with assert of HIRQ. Confirm the amount of the compression data by reading register address h35 and h34, and the error report by reading register address h36.

The processing flow chart of compression is shown since Figure 7-5-2. The example of the pixel bus of PCLK synchronous mode and the host bus of the register access mode is shown in Figure 7-5-2. The example of both of the DMA mode of the pixel bus and the host bus is shown in Figure 7-5-3. The pixel bus is PCLK synchronous mode and the host bus is register access mode in Figure 7-5-4. This example indicates the case where initializing the chip by writing the header data. Figure 7-5-5 and 7-5-6 shows the timesharing register access mode without using the Pixel bus. Figure 7-5-5 shows the DMA mode and figure 7-5-6 is register access mode.

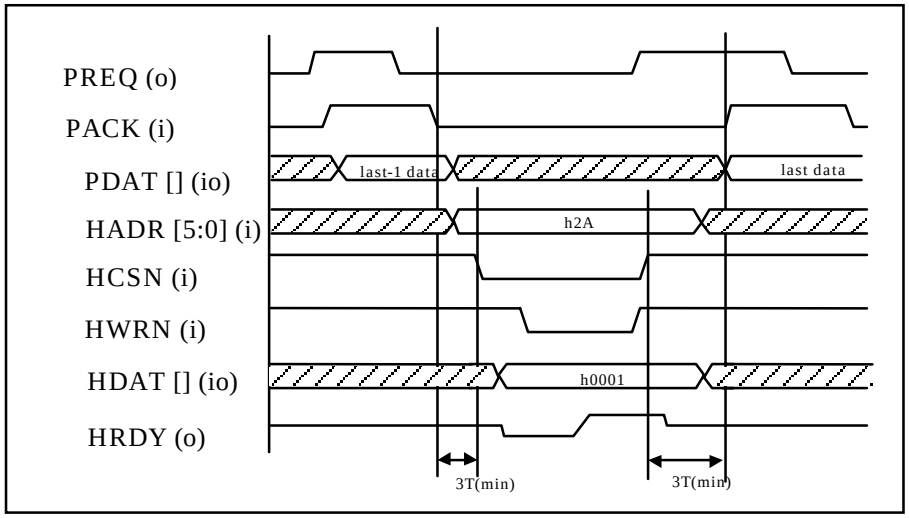


Figure 7-5-1 End command write timing

7) Control and data process flow

7.5 Compression (continued)

*Host Bus:Register access mode
*Pixel Bus : PCLK synchronous mode

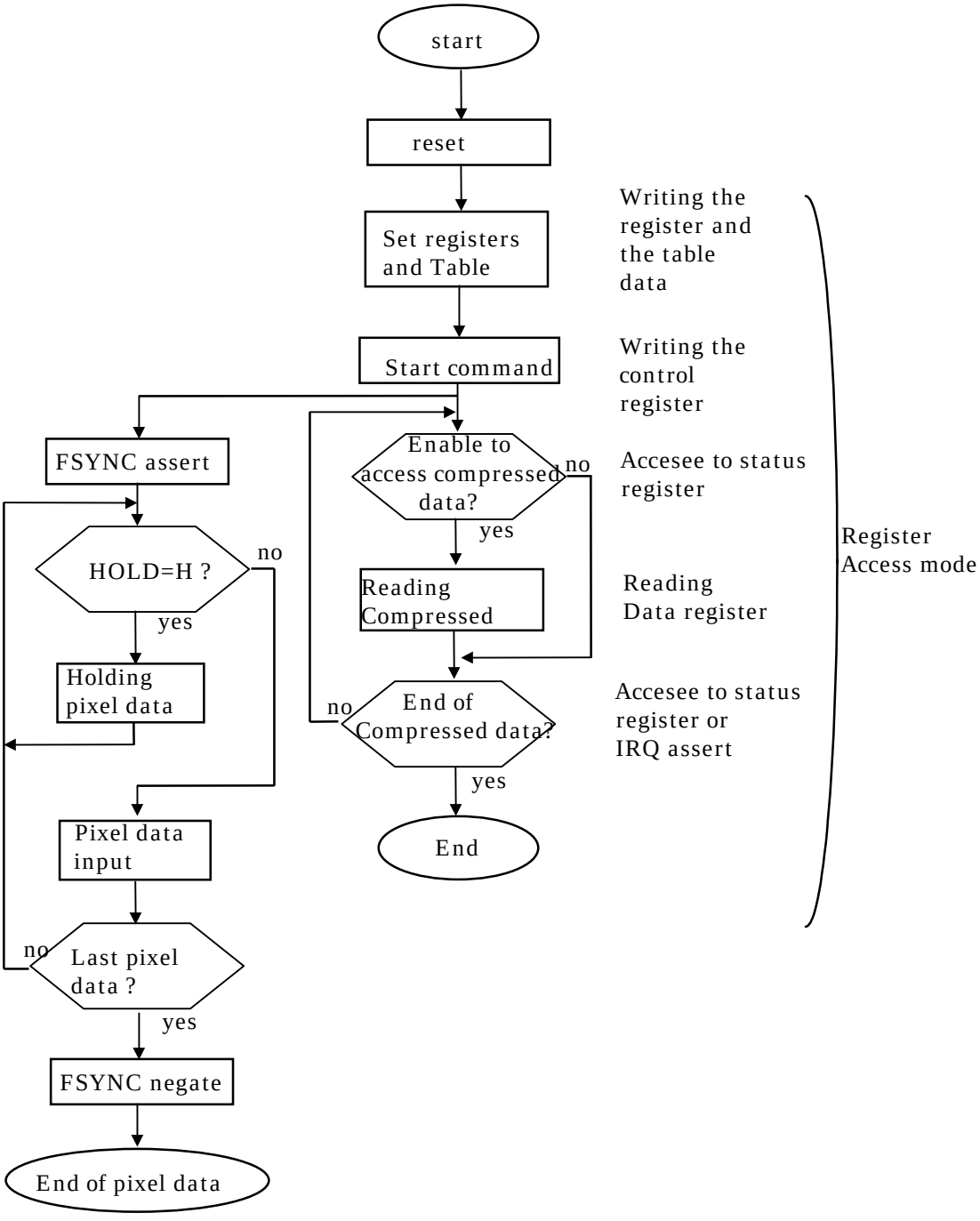


Figure 7-5-2 Register access, PCLK synchronous mode compression flow

7) Control and data process flow

7.5 compression(continued)

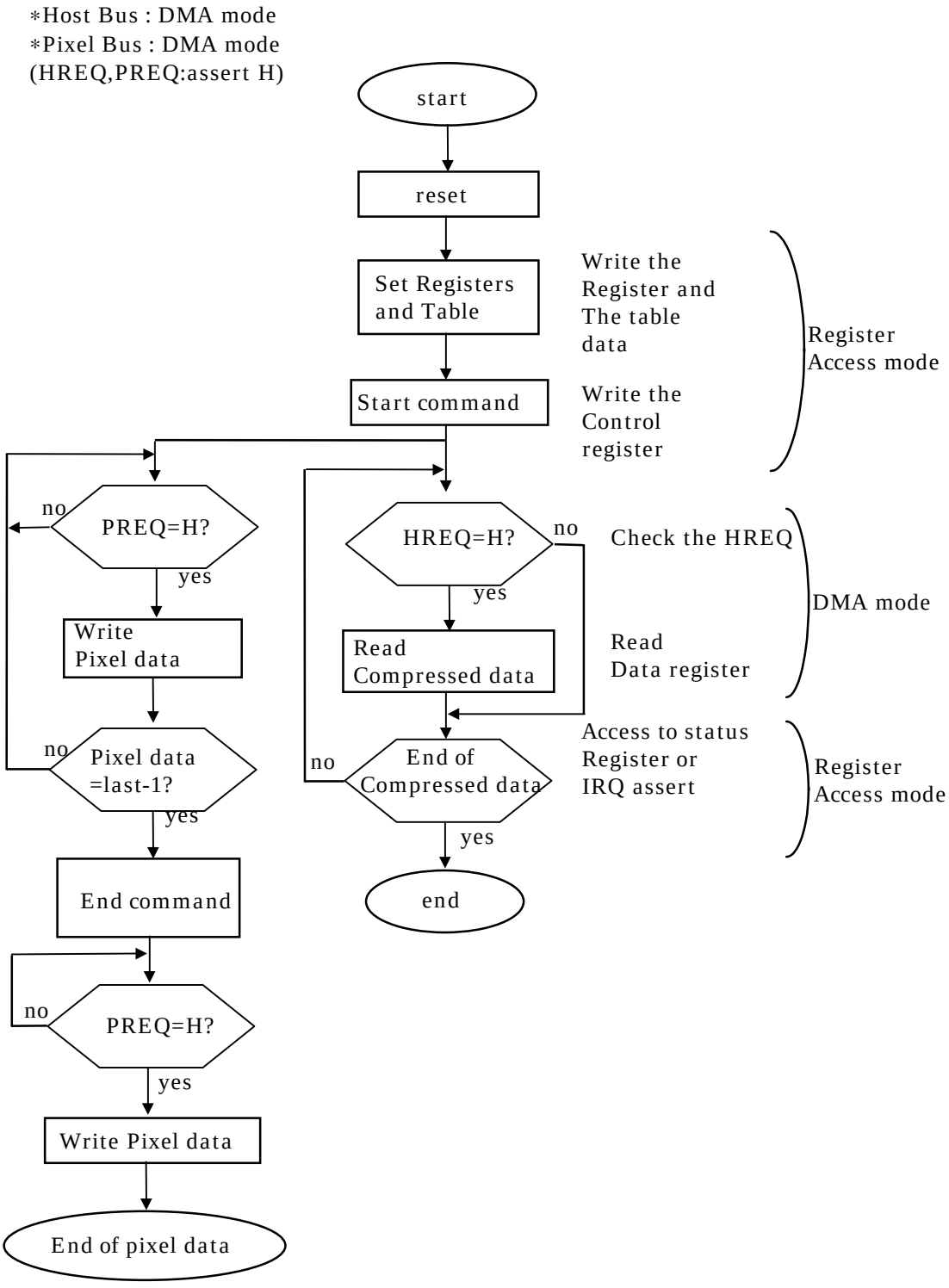


Figure 7-5-3 Host DMA, Pixel DMA compression flow

7) Control and data process flow

7.5 Compression(continued)

∗Host Bus : Register access mode and
Setting from header data
∗Pixel Bus : PCLK synchronous mode

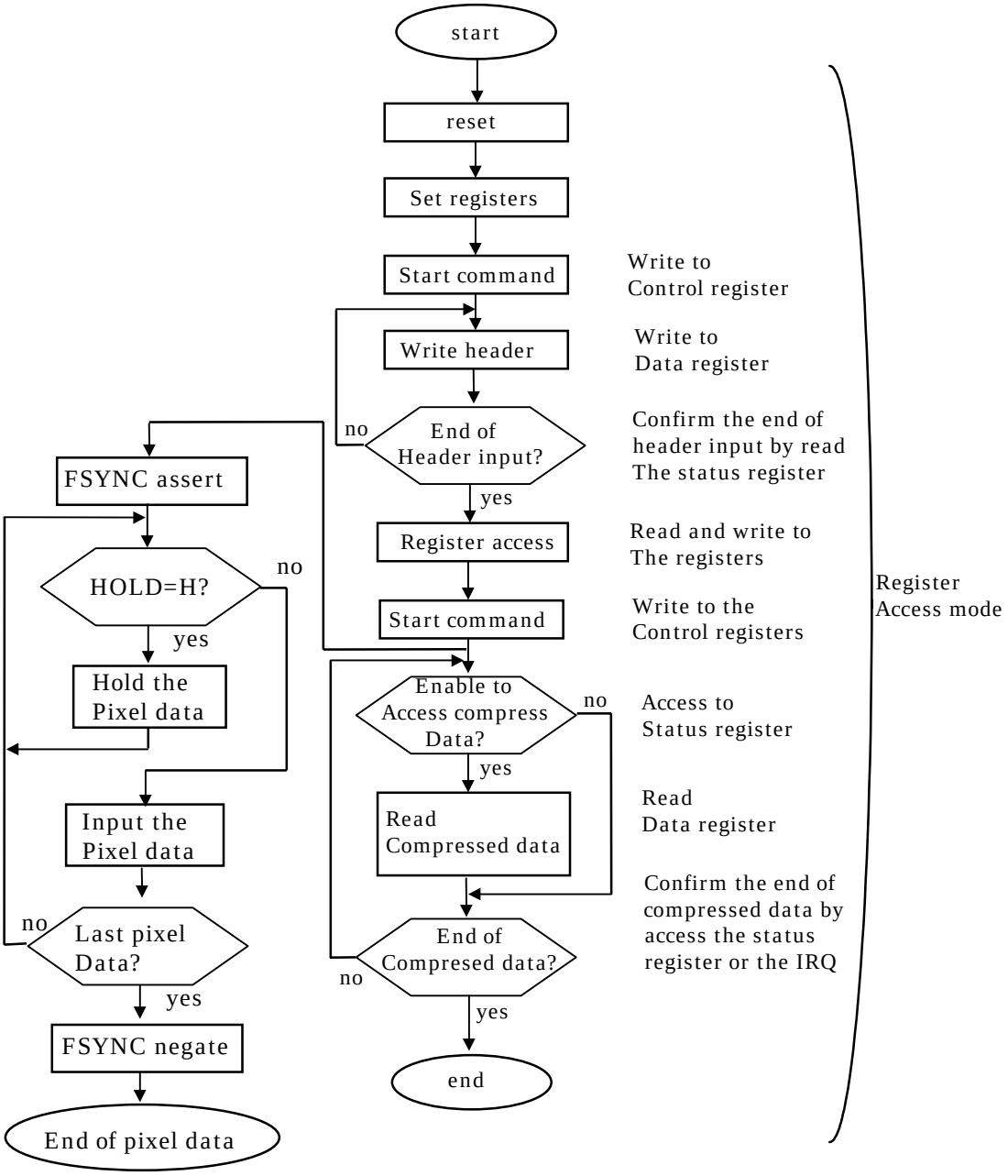


Figure 7-5-4 Initialize flow by Header data

7) Control and data process flow

7.5 compression(continued)

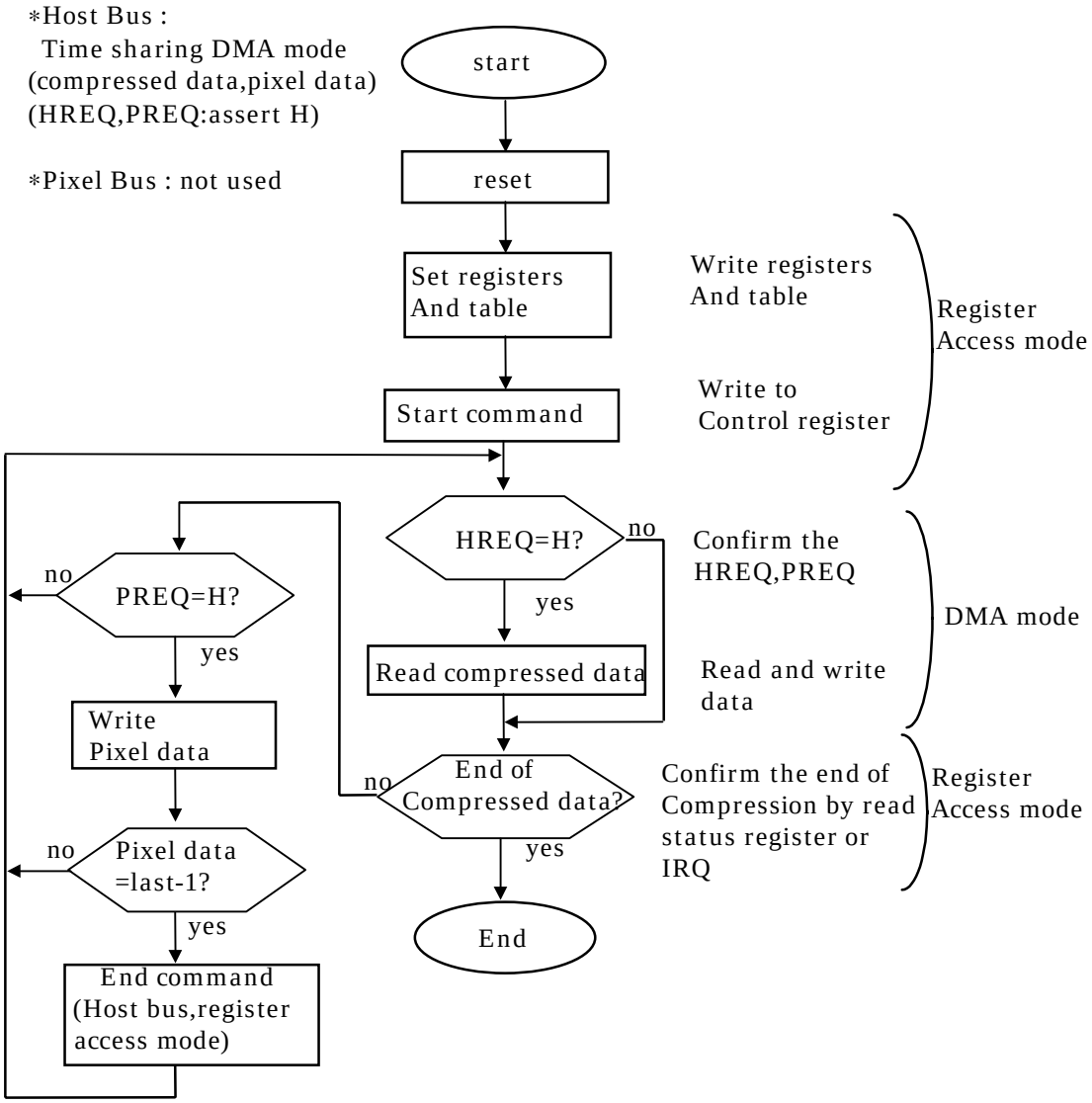


Figure 7-5-5 Time sharing DMA mode compression flow

7) Control and data process flow

7.5 Compression(continued)

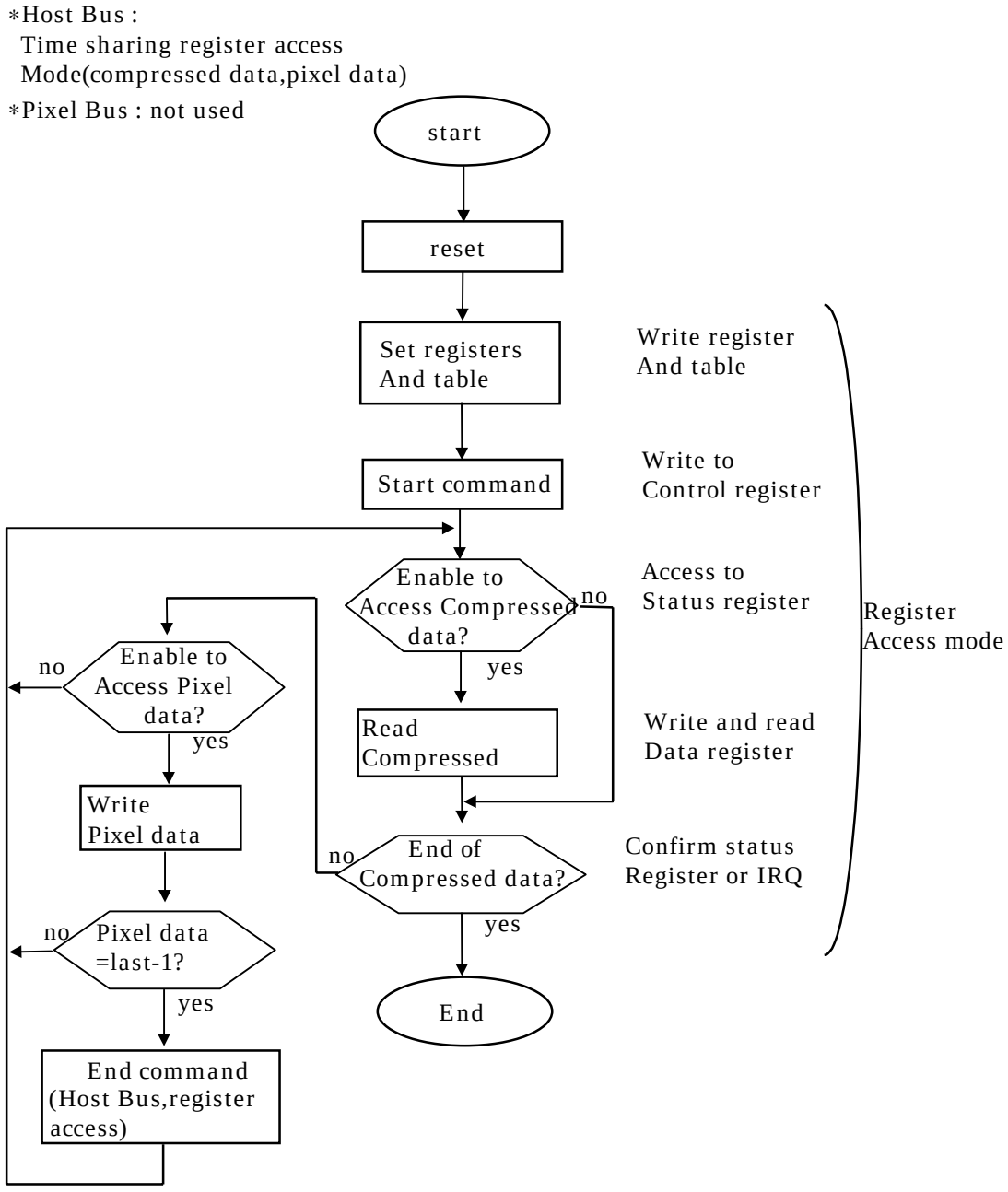


Figure 7-5-6 Time sharing register access mode compression flow

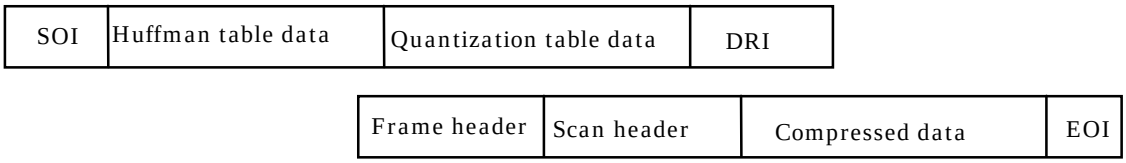
7) Control and data process flow

7.6 Data Format

The compressed data is output by the data format in accordance with the JPEG standard. Figure 7-6-1 shows the data format. In mode of without table data in the header or without using the restart maker, the data format becomes data which deletes the item which is each correspondence from this figure.

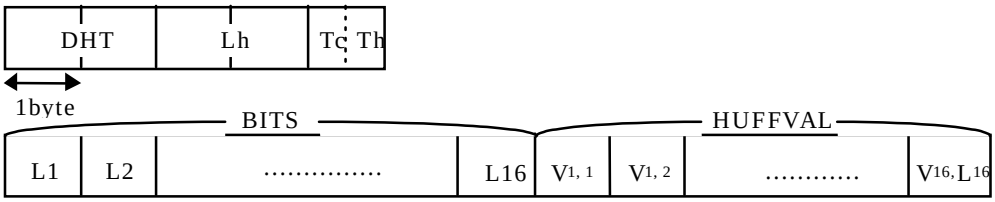
Figure 7-6-2 shows the example of the compression data. Please refer to JPEG standard (ISO/IEC10918-1) for detailed information on the data format.

Compressed data format



SOI(Start Of Image): Marks the beginning of data. Code value=hFFD8
EOI(End Of Image) : Marks the end of data. Code value=hFFD9

Huffman table data



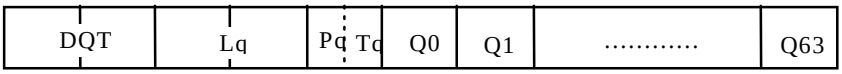
DHT(16): Marks the beginning of Huffman table data. Code value=hFFC4
Lh(16) : Number of byte in data except DHT.
Tc(4) : DC table=0、AC table=1.
Th(4) : Table number
Ln(8) : Huffman table data for Th. Specifies the number of Huffman Codes for each length.
Vij(8) : Huffman table data for Th. The elements In occurrence frequency of the order. (DC=SSSS,AC=RRRR/SSSS)

*( )The number indicates the size(bits)

Fig.7-6-1 Compressed data format

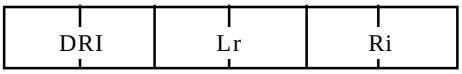
7) Control and data process flow
7.6 Data format (continued)

Quantization table data



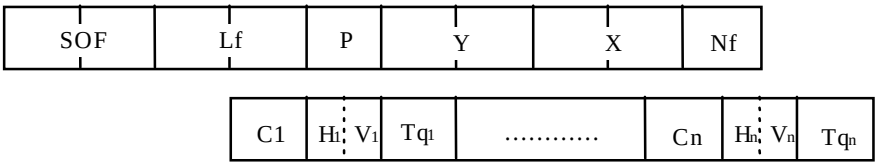
DQT(16): Marks the beginning of quantization table. Code value=hFFDB
Lq(16) : Number of byte in data except DQT.
Pq(4) : Specifies the precision of table data. The value is 0 (8bit,baseline).
Tq(4) : Table number
Qn(8) : Specifies the nth element out of 64 elements.

DRI



DRI(16) : Marks the beginning of DRI. Code value=hFFDD
Lr(16) : Number of byte in data except DRI.
Ri(8) : The number of MCU in the restart interval.

Frame header



SOF(16) : Marks the beginning of the Frame header. Code value in the baseline = hFFC0
Lf(16) : Number of byte in data except SOF.
P(8) : Precision in bits for pixel data. Value in baseline = 8
Y(16) : Number of line in frame.
X(16) : Number of samples per line.
Nf(8) : Number of image components in frame.
Cn(8) : Component identifier
Hn(4) : Horizontal sampling factor
Vn(4) : Vertical sampling factor
Tqn(8) : Quantization table selector

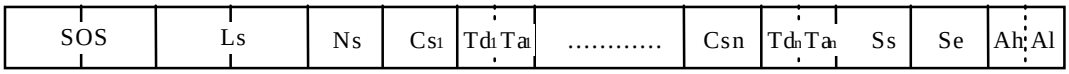
*( )The number indicates the size(bits)

Fig.7-6-1 Compressed data format (continued)

7) Control and data process flow

7.6 Data format (continued)

Scan header



SOS(16) :Marks the beginning of the Scan header. Code value = hFFDA
Ls(16) :Number of byte in data except SOS.
Ns(8) :Number of image components in scan.
Csn(8) :Scan component selector
Tdn(4) :DC Huffman table selector
Tan(4) :AC Huffman table selector
Ss(8) :Start of spectral selector. The value in baseline is 0.
Se(8) :End of spectral selector. The value in baseline is d63(h3F).
Ah(4) :The value in baseline process is 0.
Al(4) :The value in baseline process is 0.

*( )The number indicates the size(bits)

Fig.7-6-1 Compressed data format (continued)

7) Control and data process flow

7.6 Data format (continued)

This is the example of the compressed data. Our chip generate the header in this order.

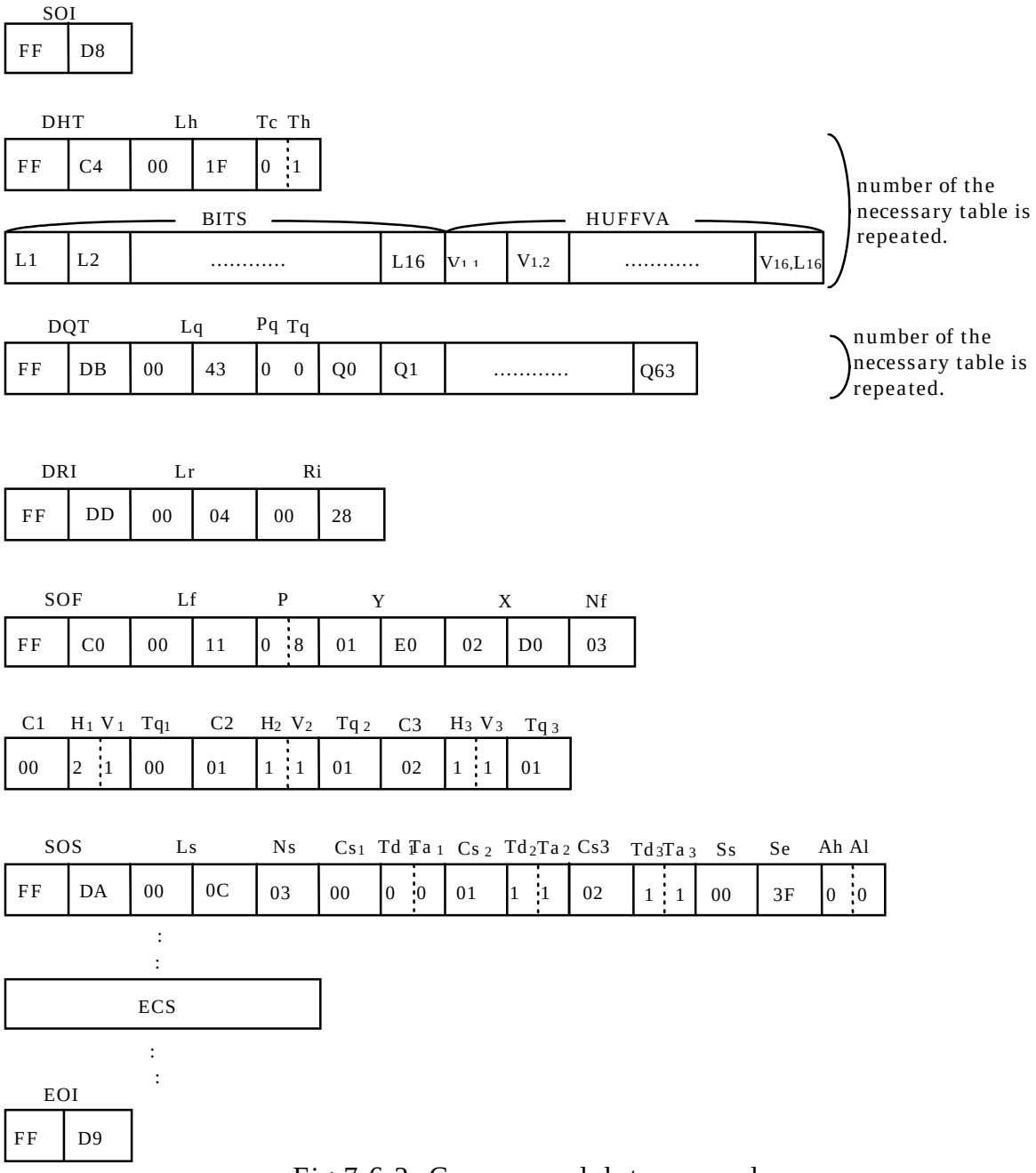


Fig.7-6-2 Compressed data example

7) Control and data process flow

7.7 De-compression

This section describes the de-compression operation with setting up described in 7.2 to 7.4. This chip will start operation when set the Start Register (register h28). If change the registers after starting the operation, This chip will not operate correctly. Register information can be read during the operation, so the status or IRQ information can be checked.

After starting this chip, the header data will be input. Write the data with asserting the HACK signal after the HREQ signal is asserted in HOST-DMA mode. In register accesses mode, write data to the compressed data register (register address = h2C) after confirming the access flag of the status register (register address = h30).

Write the compressed data after the header data, then pixel data will be output after 200-600 clock period. Latency changes according to whether the access mode and the compressed data are continuously written. In PCLK synchronous mode, the pixel data is output after asserting the FSYNC signal. In pixel DMA mode, after confirming the asserting the PREQ signal and read the pixel data with asserting the PACK signal. Read the image data from the image data register (register address = h2E) for the register access mode after confirming being able to access the register by reading the status register (register address = h30).

In host DMA mode, set the compression and the de-compression end flag (register address = h2A) after end of the data input of the previous data of the final compressed data input, and inform the chip the following data is the final compressed data. Then input the EOI code as the last data. HREQ signal is asserted after writing the last data if the end flag is not set. HREQ is negated because this chip decode EOI maker and acknowledges the end of the compression data. There is no problem if input the HREQ after the EOI code because this chip disregards the data after EOI. Refer to Figure 7-5-1 for the timing of the set of the end flag.

In the PCLK synchronous mode, after the output of the last pixel data, this chip negate the FSYNC signal and tell the completion of the output of the pixel data. In the pixel DMA mode, this chip end the asserting the PREQ signal after the last pixel data.

In the register access mode of the compressed data, set the end flag for completion of the data. If the end flag is not set, disregards the asserting the access flag. This chip knows the end of the input of the compressed data by recognizing the EOI maker. The data access flag is negated at this timing. Because data input after the EOI marker is ignored, there is no state problem same as DMA mode.

The occurrence of the error and the start of the image data output, completion can be confirmed with assert of HIRQ by setting of the IRQ flag (register address =h32). To confirm the de-compression result read the error report register, address =h36.

7) Control and data process flow

7.7 De-compression (continued)

Flow figure of de-compression is shown in the following. As for the figure 7-7-1, pixel side is when the PCLK synchronous mode, a host side is the register access mode. A figure 7-7-2 is the example of the DMA mode in both pixel side and the host side. A figure 7-7-3, a figure 7-7-4 are when either pixel bus isn't used and a host bus is used in the time sharing mode. Figure 7-7-3 is DMA, a figure 7-7-4 is register access mode.

*Host Bus : register access mode
*Pixel Bus : PCLK synchronous mode

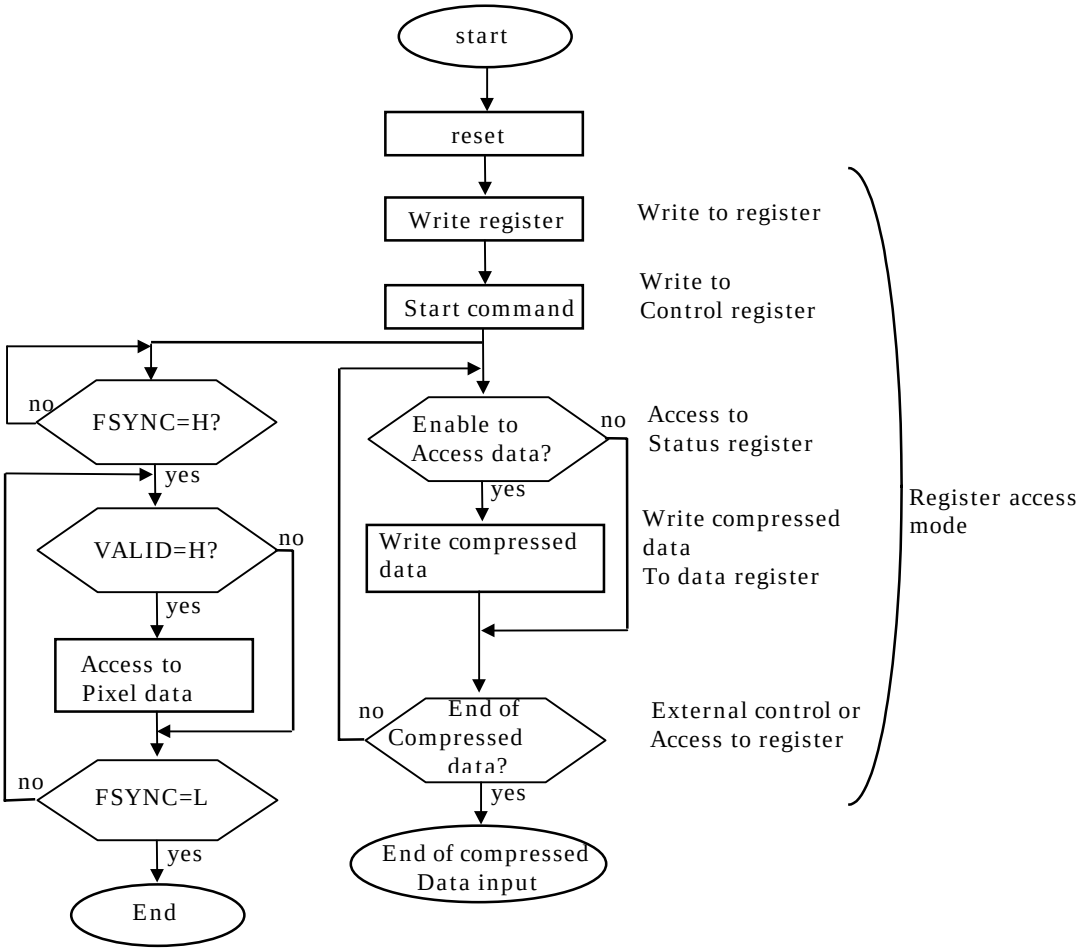


Fig.7-7-1 Register access, PCLK synchronous de-compression flow

7) Control and data process flow

7.7 De-compression (continued)

*Host Bus : DMA mode
*Pixel Bus : DMA mode
(HREQ,PREQ:assert H)

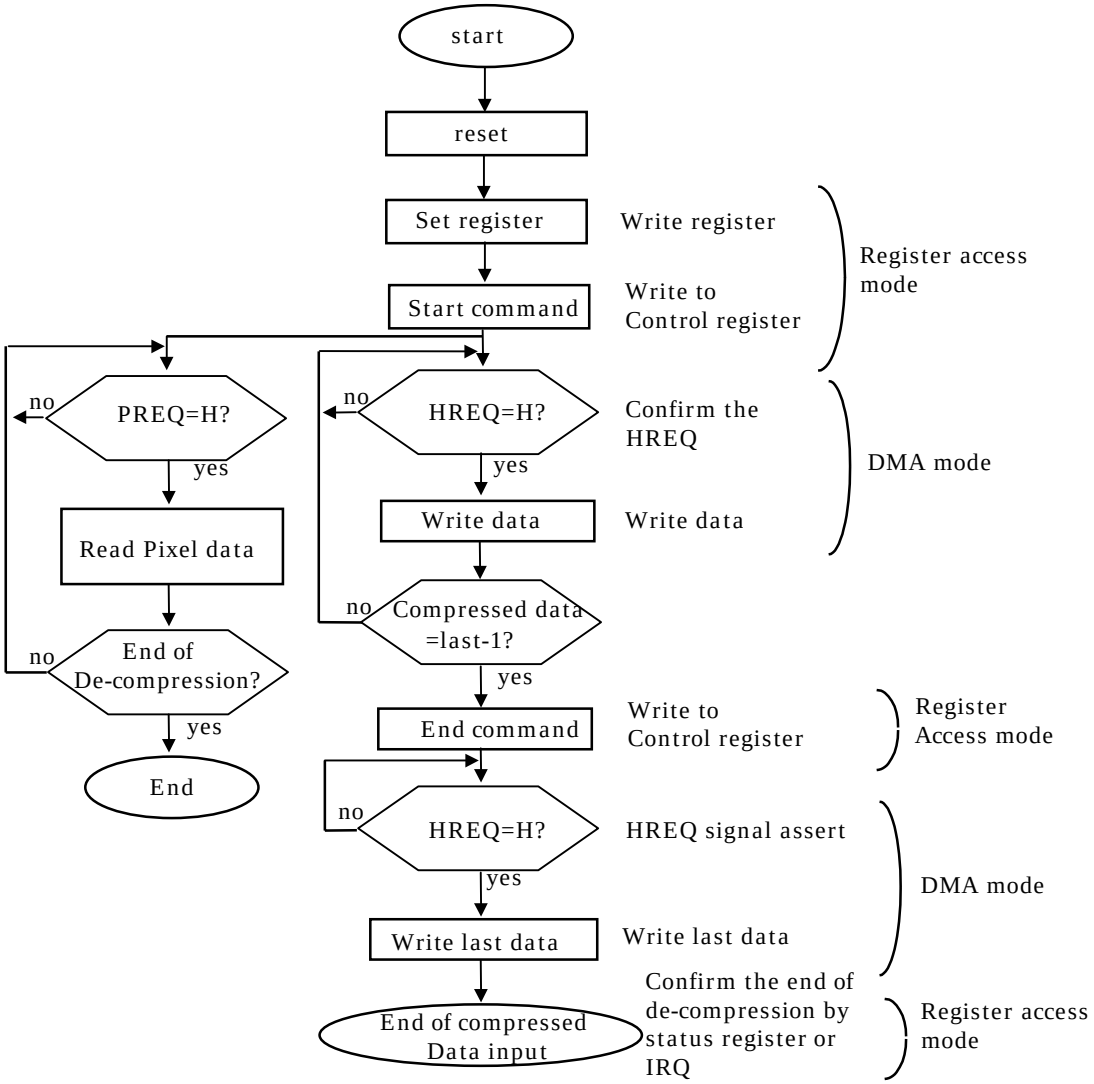


Fig.7-7-2 Host DMA、Pixel DMA de-compression flow

7) Control and data process flow

7.7 De-compression (continued)

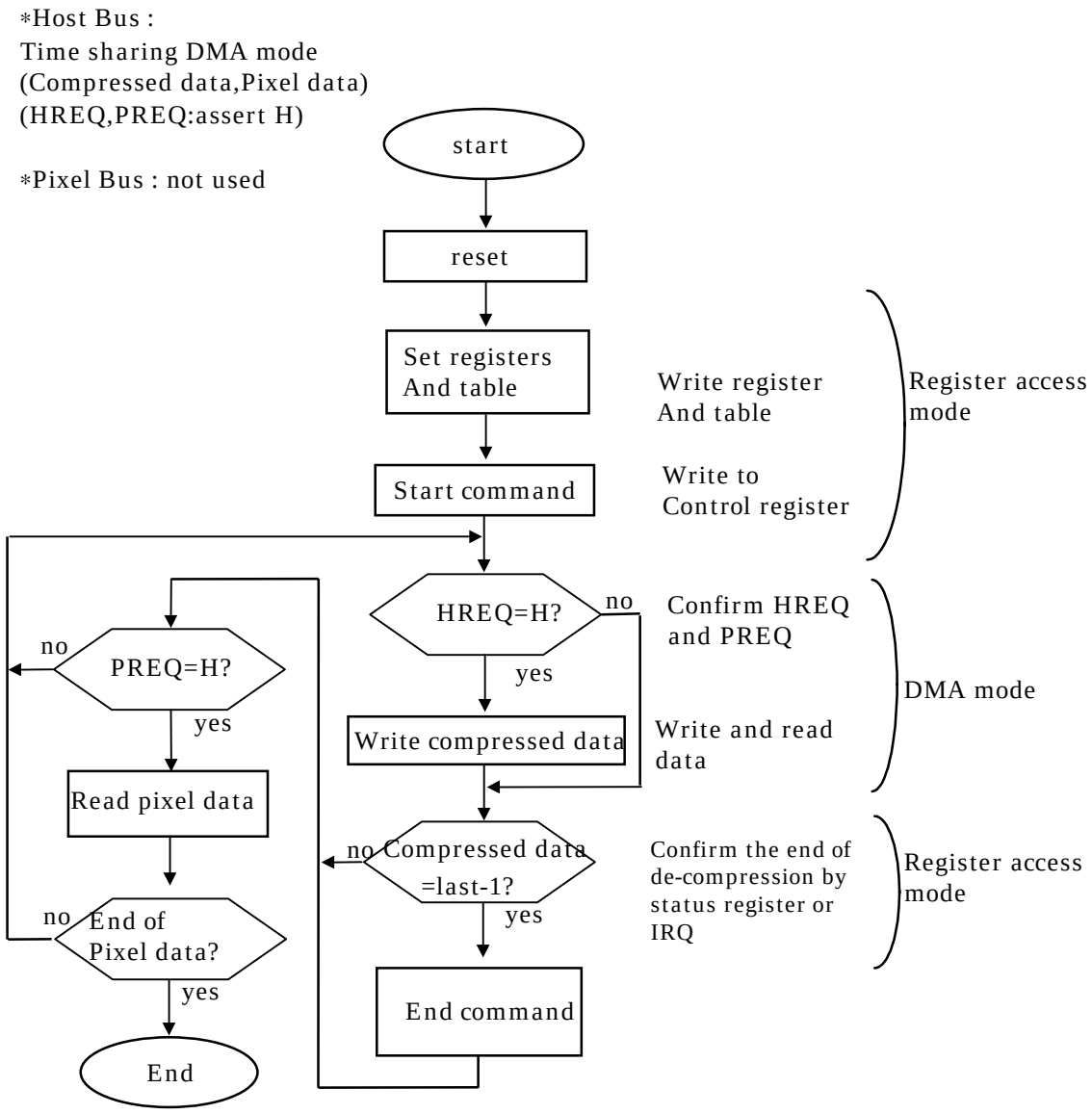


Fig.7-7-3 Time sharing DMA de-compression flow

7) Control and data process flow

7.7 De-compression (continued)

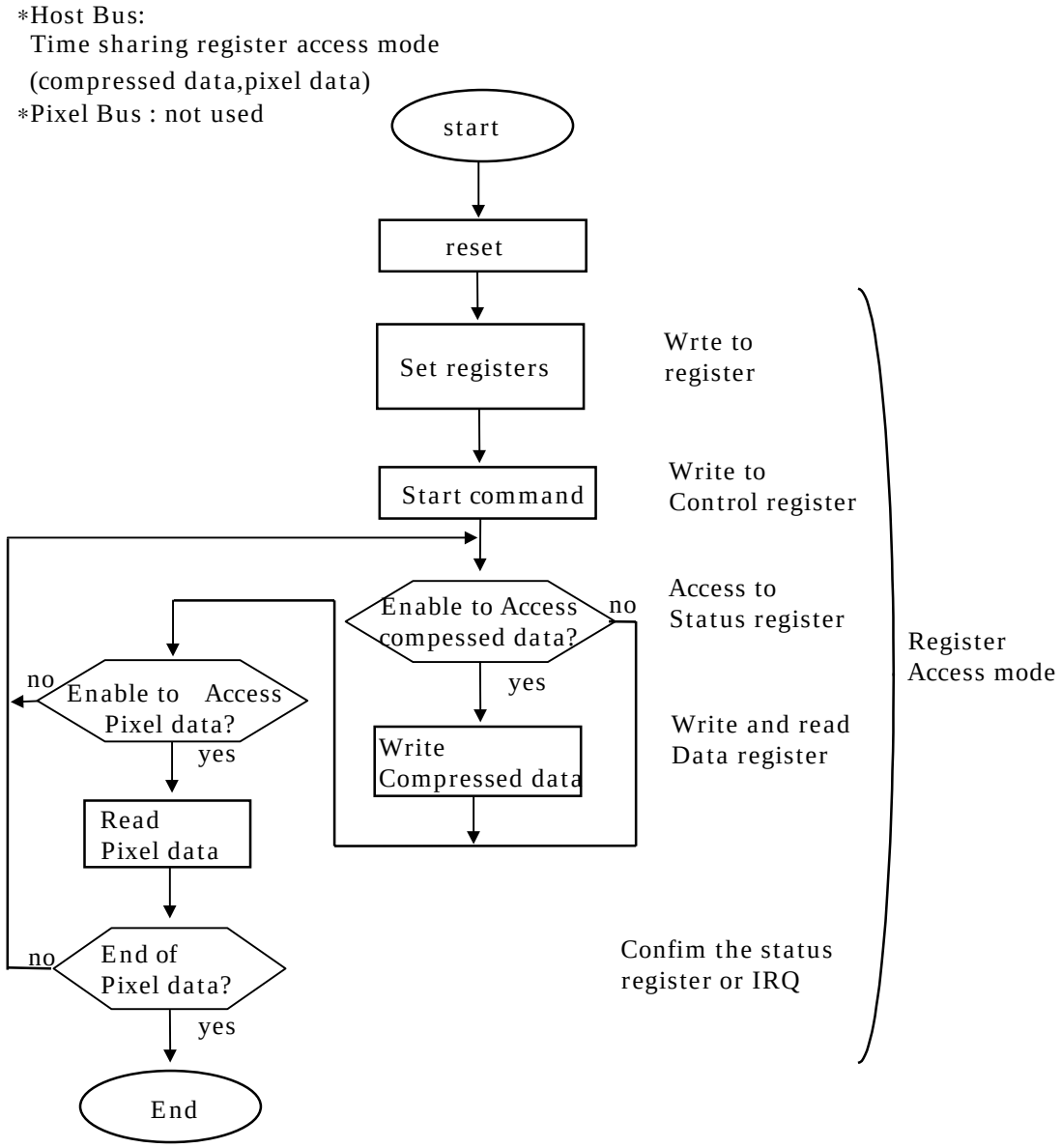


Fig.7-7-4 Time sharing register access de-compression flow

7) Control and data process flow

7.8 In data of the order

A host, a pixel bus can set up the Endian form of the data in the case of the data access by 16 bits in each of the independence. An Endian form is eight bits in word-data arrangement form (1 byte). Little Endian arranges lower address data in the byte mode on the lower byte, upper address data on the upper byte. That is reverse with Big Endian. An example in data of the order with Big Endian, Little Endian is shown in the following. It is shown with the example with Header (SOI, DQT) by the comparison with eight bits.

Little Endian

Data order	16bit MSB LSB hex (bin)	Data order	8bit MSB LSB hex (bin)
1	D8 FF (1101 1000 1111 111)	1	FF (1111 1111)
		2	D8 (1101 1000)
2	DB FF (1101 1011 1111 1111)	3	FF (1111 1111)
		4	DB (1101 1011)
3	43 00 (0100 0011 0000 0000)	5	00 (0000 0000)
		6	43 (0100 0011)

Table 7-8-1 Little Endian data order

Big Endian

Data order	16bit MSB LSB hex (bin)	Data order	8bit MSB LSB hex (bin)
1	FF D8 (1111 111 1101 1000)	1	FF (1111 1111)
		2	D8 (1101 1000)
2	FF DB (1111 1111 1101 1011)	3	FF (1111 1111)
		4	DB (1101 1011)
3	00 43 (0000 0000 0100 0011)	5	00 (0000 0000)
		6	43 (0100 0011)

Table 7-8-2 Big Endian data order

7) Control and data process flow

7.9 Examples of setting up registers

Pixel data : YUV4:2:2, 640x480 pixel
compressed data : Interchange format
Host Bus : 16 bits little endian
Pixel Bus : 16 bits little endian
Bus Access : Host DMA mode, Pixel individual DMA mode
Active level : HREQ, HACK, PREQ, PACK and HIRQ are active H.
Data Volume Limit : 256 K bytes
Restart Interval : 40 MCU
DQT identifier : Y=0, UV=1
DHT identifier : Y=0, UV=1
HIRQ assert condition : last data output end, overflow compressed data limit, error occur

Address (hex)	Value	Function
00	0005	Bus definition is 16 bits and little endian.
02	001F	HREQ, HACK, PREQ, PACK and HIRQ are active H.
04	0001	PDAT use
06	0057	DMA mode, data output enable, header information loading by registers, compression
08	0100	the limit of compressed data volume is 256 K bytes
0A	000C	normal output, with DHT and DQT
12	0028	DRI=40MCU
14	01E0	Y=480 lines
16	0280	X=640 pixels per line
18	001B	Nf=Ns=3 components
1A	0600	Tq1=0, H1=2, V1=1, C1=0
1C	1501	Tq2=1, H2=1, V2=1, C2=1
1E	1502	Tq3=1, H3=1, V3=1, C3=2
22	0ED0	Cs1=C1, Td1=Ta1=0 Cs2=C2, Td2=Ta2=1 Cs3=C3, Td3=Ta3=1
32	00E0	HIRQ is asserted when last data output end, overflow compressed data limit, error occur.

Table 7-9-1 An example of setting up registers in compression

7) Control and data process flow

7.9 Examples of setting up registers

Address (hex)	Value	Function
00	0005	Bus definition is 16 bits and little endian.
02	001F	HREQ, HACK, PREQ, PACK and HIRQ are active H.
04	0001	PDAT use
06	0056	DMA mode, data output enable, header information loading by registers, decompression
32	00E0	HIRQ is asserted when last data output end, overflow compressed data limit, error occur.

In decompression, most parameters are loaded by header of compressed data.

Table 7-9-2 An example of setting up registers in decompression

7) Control and data process flow

7.10 Outlines of frame operation time

Outlines of flame operation time are indicated below. The flame size is 640x480 pixels and the format is YUV4:2:2. "T" means system clock period. The value shown in a parenthesis is time in case 32 MHz system clock rate. In this examples, Pixel Bus is 16 bits width and accessed by PCLK synchronous mode, and Host Bus is 16 bits width and accessed by DMA mode, and There are no interruptions from external systems. Input or output time for header can be changed by header parameters for example number of tables.

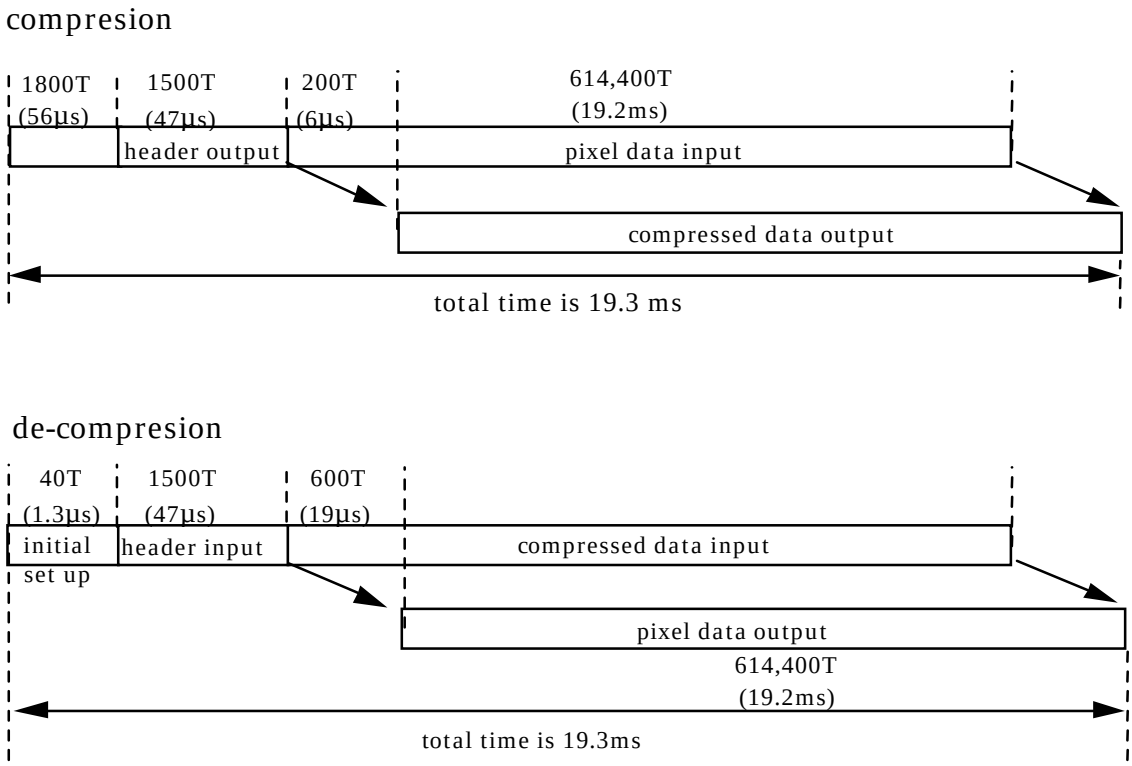


Fig.7-10-1 frame operation time example

8) Electrical Characteristics (DC)

8.1 Absolute Maximum Ratings

No.	Parameter	Symbol	Limit	Unit
1	DC Supply Voltage	VDD	-0.3 - +0.4	V
2	Input Voltage	VIN	-0.3 - VDD+0.3	V
3	DC Output Current	IOUT	±15	mA
4	Storage Temperature	TSTG	-55 - +125	°C

8.2 Recommended Operating Conditions

No.	Parameter	Symbol	Limit	Unit
5	DC Supply Voltage	VDD	3.0 - 3.6	V
6	Ambient Temperature	Ta	0 - +70	°C

8.3 DC Characteristics (under Recommended Operating Conditions)

No.	Parameter	Symbol	Test Condition	Min	Max	Unit
7	Input Low Voltage	VIL		—	0.8	V
8	Input High Voltage	VIH		2.0	3.9	V
9	Output Low Voltage	VOL	IOL = +4mA	—	0.4	V
10	Output High Voltage	VOH	IOL = -4mA	2.4	—	V
11	Input Leakage Current	IIL	VIN = GND	-10	—	µA
12	Input Leakage Current	IIH	VIN = VDD	—	10	µA
13	Output Leakage Current	IOZ	At 3-state Output	-10	10	µA
14	Quiescent Supply Current	IDDS	VIN = VDD or GND	—	100	µA
15	Dynamic Supply Current	IDDOP	Output Capacitance = 50pF & Internal f =32MHz	—	140	mA
16	Supply Current at LOWPWR	IDDLP	LOWPWR = H VIN = VDD or GND (except PCLK)	—	1.2	mA
				850(typical)		µA
17	Input Capacitance	CIN	f = 1MHz, VIN = GND, v in = 100 mVrms	—	15	PF
18	Output Capacitance	COUT		—	15	PF

9) Electrical Characteristics (AC)

9.1 PCLK

The maximum frequency at PCLK input using PLL is the half of not using PLL. Even if PLL is in use or not, the maximum through-put is the same. Because Internal PCLK signal is made twice as fast as PCLK input in the case of using PLL.

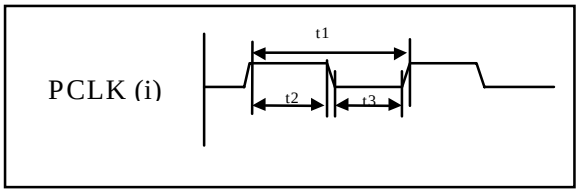


Figure 9-1-1 PCLK timings

Symbol	Parameter	Min	Max	Unit	Conditions
t1	PCLK Cycle Time	31.25	-	ns	PLL is not in use.
		62.5	83	ns	PLL is in use.
t2	PCLK Pulse Width High	15	-	ns	PLL is not in use.
		30	42	ns	PLL is in use.
t3	PCLK Pulse Width Low	15	-	ns	PLL is not in use.
		30	42	ns	PLL is in use.
-	Lock Time	-	2	ms	PLL is in use.

Table 9-1-2 AC Characteristics-PCLK input

9.2 Host Bus register access mode (write)

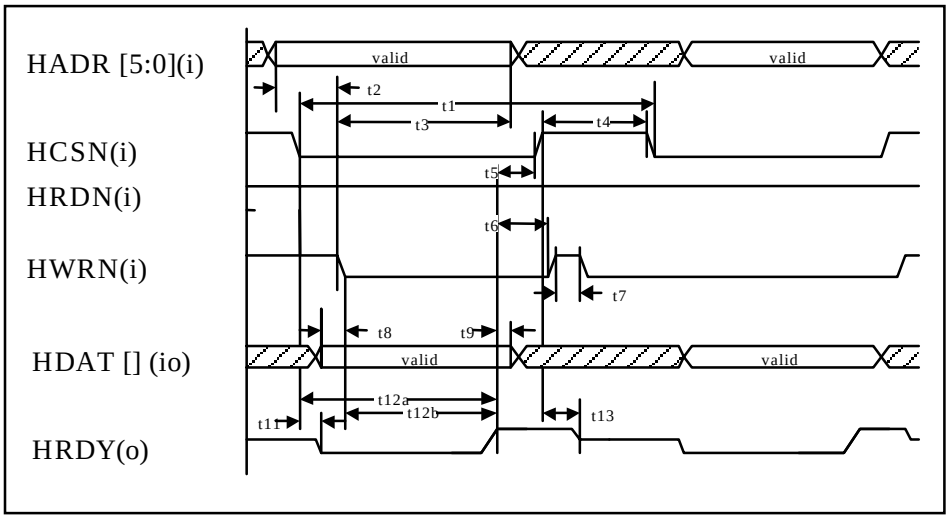


Figure 9-2-1 Host Bus (register access) write timing

Symbol	Parameter	Min	Max	Unit	Conditions
t1	HCSN Write Cycle	6T	-	ns	
t2	HADR Setup Time (HWRN Fall)	-12	-	ns	*1
t3	HADR Hold Time (HWRN Fall)	3T	-	ns	
t4	HCSN Negate Width	1.5T	-	ns	
t5	HCSN Hold Time (HRDY Rise)	0	-	ns	
t6	HWRN Hold Time (HRDY Rise)	0	-	ns	
t7	HWRN Negate Width	1.5T	-	ns	
t8	HDAT Setup Time (HWRN Fall)	-12	-	ns	*2
t9	HDAT Hold Time (HRDY Rise)	0	-	ns	
t11	HCSN Assert - HRDY L Output Delay	-	18	ns	Output Loading is 50pF.
t12	If both HCSN and HWRN are asserted, WRITE cycle will begin.				
t12a	HCSN Assert - HRDY Assert	-	3.5T	ns	Output Loading is 50pF.
t12b	HWRN Assert - HRDY Assert	-	3.5T	ns	Output Loading is 50pF.
t13	HCSN Negate - HRDY 3-State Delay	-	18	ns	Output Loading is 50pF.

Note: *1 A valid data delay on HADR is admitted 12ns from assert of HWRN.

*2 A valid data delay on HDAT is admitted 12ns from assert of HWRN.

Table 9-2-2 AC Characteristics-Host Bus (register access) write mode

9.3 Host Bus register access mode (read)

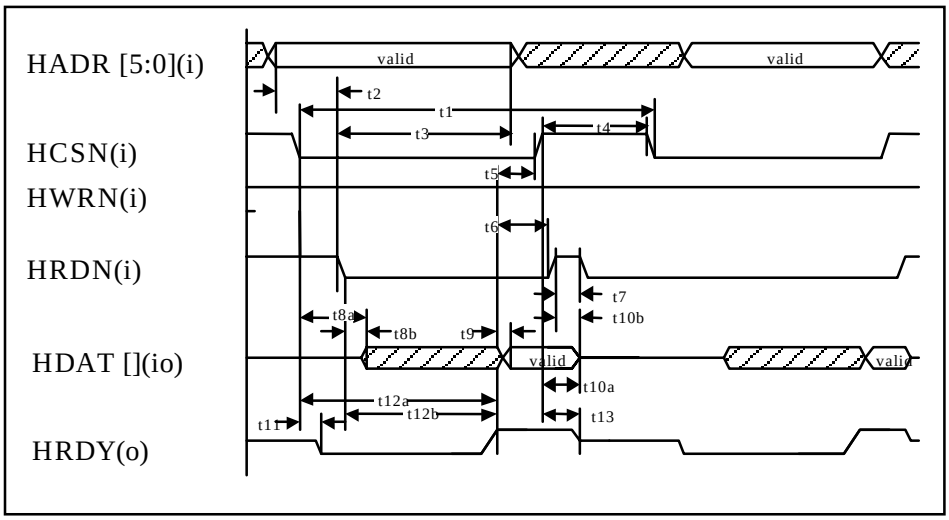


Figure 9-3-1 Host Bus (register access) read timing

Symbol	Parameter	Min	Max	Unit	Conditions
t1	HCSN Read Cycle	6T	-	ns	
t2	HADR Setup Time (HRDN Fall)	-12	-	ns	*1
t3	HADR Hold Time (HRDN Fall)	3T	-	ns	
t4	HCSN Negate Width	1.5T	-	ns	
t5	HCSN Hold Time (HRDY Rise)	0	-	ns	
t6	HRDN Hold Time (HRDY Rise)	0	-	ns	
t7	HRDN Negate Width	0.5T	-	ns	
t8	If both HCSN and HRDN are asserted, HDAT will be on output state.				
t8a	HCSN Assert - HDAT Output Delay	-	18	ns	Output Loading is 50pF.
t8b	HRDN Assert - HDAT Output Delay	-	18	ns	Output Loading is 50pF.
t9	HRDY Assert - HDAT Valid Data Output Delay	-	5	ns	Output Loading is 50pF.
t10	If HCSN or HRDN is negated, HDAT will be on 3-state.				
t10a	HCSN Negate - HDAT 3-state Delay	-	18	ns	Output Loading is 50pF.
t10b	HRDN Negate - HDAT 3-state Delay	-	18	ns	Output Loading is 50pF.
t11	HCSN Assert - HRDY L Output Delay	-	18	ns	Output Loading is 50pF.
t12	If both HCSN and HRDN are asserted, READ cycle will begin.				
t12a	HCSN Assert - HRDY Assert	-	3.5T	ns	Output Loading is 50pF.
t12b	HRDN Assert - HRDY Assert	-	3.5T	ns	Output Loading is 50pF.
t13	HCSN Negate - HRDY 3-State Delay	-	18	ns	Output Loading is 50pF.

Note: *1 A valid data delay on HADR is admitted 12ns from assert of HRDN.

Table 9-3-2 AC Characteristics-Host Bus (register access) read mode

9.4 Host Bus register access (writing the table data continually) mode

In Host Bus register access (writing the table data continually) mode, admitted write data is only table data. For the mode specification, please use the table data address (h10), then other writing for specification with other address is not necessary. In other mode, Host Bus register access is the usual writing sequence (show 9.2). The table data address is write only but not readable.

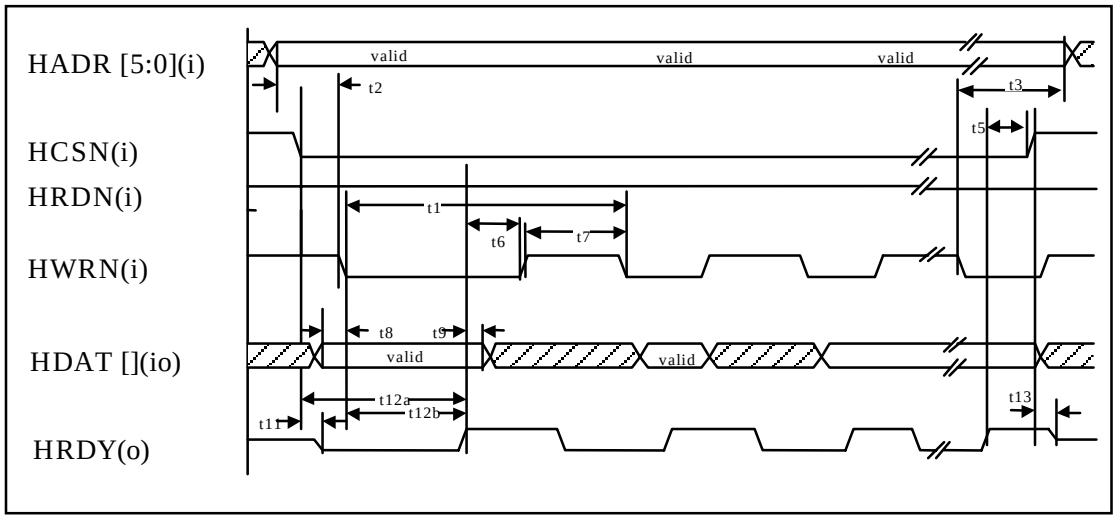


Figure 9-4-1 Host Bus register access (writing the table data continually) timing

Symbol	Parameter	Min	Max	Unit	Conditions
t1	HWRN Write Cycle	4T	-	ns	
t2	HADR Setup Time (HWRN Fall)	-12	-	ns	*1
t3	HADR Hold Time (HWRN Fall)	3T	-	ns	
t4	HCSN Negate Width	1.5T	-	ns	
t5	HCSN Hold Time (HRDY Rise)	0	-	ns	
t6	HWRN Hold Time (HRDY Rise)	0	-	ns	
t7	HWRN Negate Width	1.5T	-	ns	
t8	HDAT Setup Time (HWRN Fall)	-12	-	ns	*2
t9	HDAT Hold Time (HRDY Rise)	0	-	ns	
t11	HCSN Assert - HRDY L Output Delay	-	-18	ns	Output Loading is 50pF.
t12	If both HCSN and HWRN are asserted, WRITE cycle will begin.				
t12a	HCSN Assert - HRDY Assert	-	3.5T	ns	Output Loading is 50pF.
t12b	HWRN Assert - HRDY Assert	-	3.5T	ns	Output Loading is 50pF.
t13	HCSN Negate - HRDY 3-State Delay	-	18	ns	Output Loading is 50pF.

Note: *1 A valid data delay on HADR is admitted 12ns from assert of HWRN.

*2 A valid data delay on HDAT is admitted 12ns from assert HWRN.

Table 9-4-2 AC Characteristics-Host Bus register access (writing the table data continually) mode

9.5 Host Bus DMA mode (the compression controlled by HWRN and HRDN)

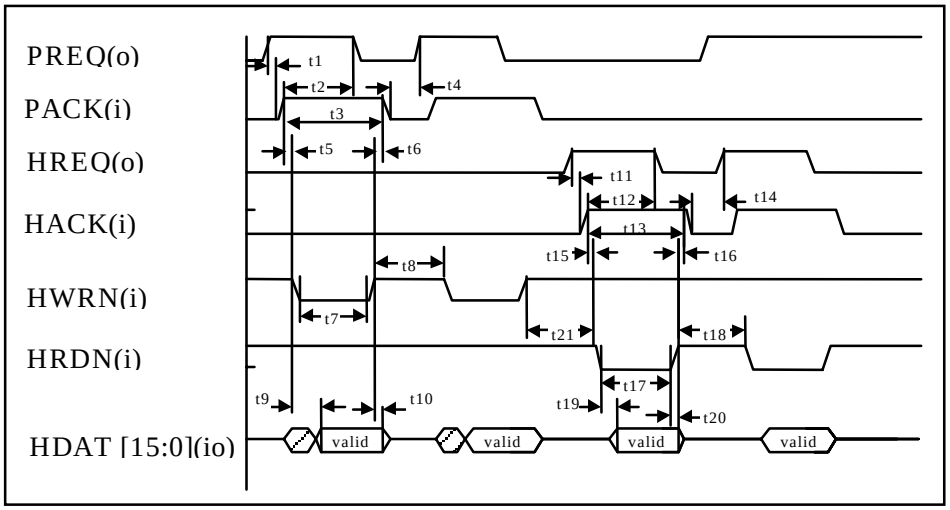


Figure 9-5-1 Host Bus DMA timing (the compression controlled by HWRN and HRDN)

Symbol	Parameter	Min	Max	Unit	Conditions
t1	PREQ Assert - PACK Assert	0	-	ns	
t2	PACK Assert - PREQ Negate	0.5T	2.5T	ns	Output Loading is 50pF.
t3	PACK Assert Width	2T	-	ns	
t4	PACK Negate - PREQ Assert	2T	-	ns	Output Loading is 50pF.
t5	HWRN Setup Time (PACK Assert)	0	-	ns	
t6	HWRN Hold Time (PACK Negate)	0	-	ns	
t7	HWRN Assert Width	2T	-	ns	
t8	HWRN Negate Width	2T	-	ns	
t9	HDAT Setup Time (HWRN Assert)	-12	-	ns	*1
t10	HDAT Hold Time (HWRN Negate)	0	-	ns	
t11	HREQ Assert - HACK Assert	0	-	ns	
t12	HACK Assert - HREQ Negate	0.5T	2.5T	ns	Output Loading is 50pF.
t13	HACK Assert Width	2T	-	ns	
t14	HACK Negate - HREQ Assert	2T	-	ns	Output Loading is 50pF.
t15	HRDN Setup Time (HACK Assert)	0	-	ns	
t16	HRDN Hold Time (HACK Negate)	0	-	ns	
t17	HRDN Assert Width	2T	-	ns	
t18	HRDN Negate Width	2T	-	ns	
t19	HRDN Assert - HDAT Output Delay	-	18	ns	When Compression Data are out. Output Loading is 50pF.
t20	HRDN Negate - HDAT 3-state Delay	-	18	ns	When Compression Data are out. Output Loading is 50pF.

Note: *1 A valid data delay on HDAT is admitted 12ns from assert of HWRN.

Table 9-5-2 AC characteristics-Host Bus DMA mode (the compression controlled by HWRN and HRDN)

9.6 Host Bus DMA mode (the compression controlled by HACK and PACK)

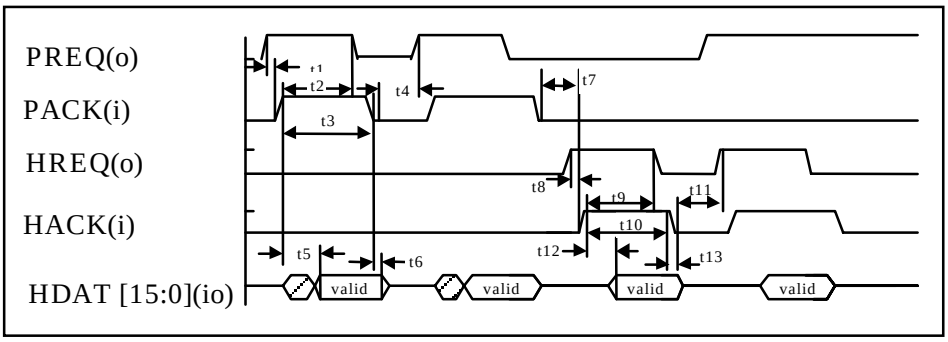


Figure 9-6-1 Host Bus DMA timing (the compression controlled by HACK and PACK)

Symbol	Parameter	Min	Max	Unit	Conditions
t1	PREQ Assert - PACK Assert	0	-	ns	
t2	PACK Assert - PREQ Negate	0.5T	2.5T	ns	Output Loading is 50pF.
t3	PACK Assert Width	2T	-	ns	
t4	PACK Negate - PREQ Assert	2T	-	ns	Output Loading is 50pF.
t5	HDAT Setup Time (PACK Assert)	-12	-	ns	*1
t6	HDAT Hold Time (PACK Negate)	0	-	ns	
t7	PACK Negate - HACK Assert	2T	-	ns	
t8	HREQ Assert - HACK Assert	0	-	ns	
t9	HACK Assert - HREQ Negate	0.5T	2.5T	ns	Output Loading is 50pF.
t10	HACK Assert Width	2T	-	ns	
t11	HACK Negate - HREQ Assert	2T	-	ns	Output Loading is 50pF.
t12	HACK Assert - HDAT Output Delay	-	18	ns	When Compression Data are out. Output Loading is 50pF.
t13	HACK Negate - HDAT 3-state Delay	-	18	ns	When Compression Data are out. Output Loading is 50pF.

Note: *1 A valid data delay on HDAT is admitted 12ns from assert of PACK.

Table 9-6-2 AC characteristics-Host Bus DMA mode (the compression controlled by HACK and PACK)

9.7 Host Bus DMA mode (the decompression controlled by HWRN and HRDN)

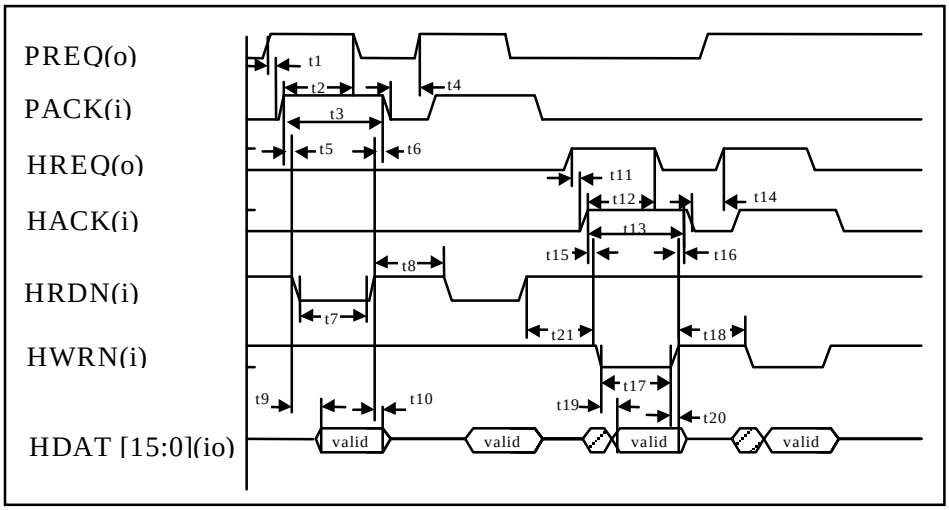


Figure 9-7-1 Host Bus DMA timing (the decompression controlled by HWRN and HRDN)

Symbol	Parameter	Min	Max	Unit	Conditions
t1	PREQ Assert - PACK Assert	0	-	ns	
t2	PACK Assert - PREQ Negate	0.5T	2.5T	ns	Output Loading is 50pF.
t3	PACK Assert Width	2T	-	ns	
t4	PACK Negate - PREQ Assert	2T	-	ns	Output Loading is 50pF.
t5	HRDN Setup Time (PACK Assert)	0	-	ns	
t6	HRDN Hold Time (PACK Negate)	0	-	ns	
t7	HRDN Assert Width	2T	-	ns	
t8	HRDN Negate Width	2T	-	ns	
t9	HRDN Assert - HDAT Output Delay	-	18	ns	When Pixel Data are out. Output Loading is 50pF.
t10	HRDN Negate - HDAT 3-state Delay	-	18	ns	When Pixel Data are out. Output Loading is 50pF.
t11	HREQ Assert - HACK Assert	0	-	ns	
t12	HACK Assert - HREQ Negate	0.5T	2.5T	ns	Output Loading is 50pF.
t13	HACK Assert Width	2T	-	ns	
t14	HACK Negate - HREQ Assert	2T	-	ns	Output Loading is 50pF.
t15	HWRN Setup Time (HACK Assert)	0	-	ns	
t16	HWRN Hold Time (HACK Negate)	0	-	ns	
t17	HWRN Assert Width	2T	-	ns	
t18	HWRN Negate Width	2T	-	ns	
t19	HDAT Setup Time (HWRN Assert)	-12	-	ns	*1
t20	HDAT Hold Time (HWRN Negate)	0	-	ns	

Note: *1 A valid data delay on HDAT is admitted 12ns from assert of HWRN.

Table 9-7-2 AC characteristics-Host Bus DMA mode (the decompression controlled by HWRN and HRDN)

9.8 Host Bus DMA mode (the decompression controlled by HACK and PACK)

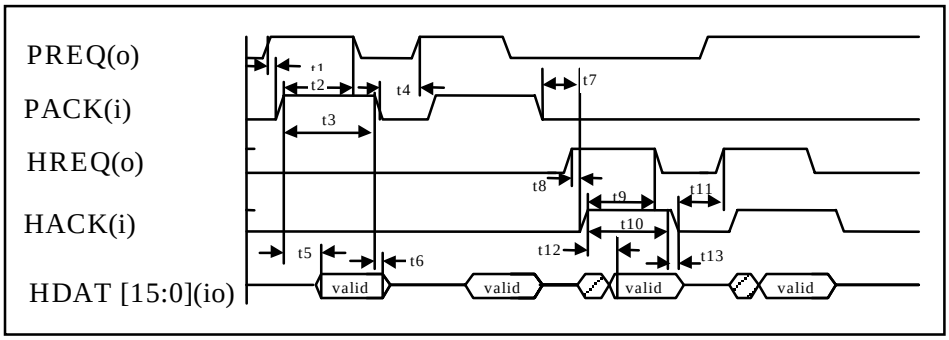


Figure 9-8-1 Host Bus DMA timing (the decompression controlled by HACK and PACK)

Symbol	Parameter	Min	Max	Unit	Conditions
t1	PREQ Assert - PACK Assert	0	-	ns	
t2	PACK Assert - PREQ Negate	0.5T	2.5T	ns	Output Loading is 50pF.
t3	PACK Assert Width	2T	-	ns	
t4	PACK Negate - PREQ Assert	2T	-	ns	Output Loading is 50pF.
t5	PACK Assert - HDAT Output Delay	-	18	ns	When Pixel Data are out. Output Loading is 50pF.
t6	PACK Negate - HDAT 3-state Delay	-	18	ns	When Pixel Data are out. Output Loading is 50pF.
t7	PACK Negate - HACK Assert	2T	-	ns	
t8	HREQ Assert - HACK Assert	0	-	ns	
t9	HACK Assert - HREQ Negate	0.5T	2.5T	ns	Output Loading is 50pF.
t10	HACK Assert Width	2T	-	ns	
t11	HACK Negate - HREQ Assert	2T	-	ns	Output Loading is 50pF.
t12	HDAT Setup Time (HACK Assert)	-12	-	ns	*1
t13	HDAT Hold Time (HACK Negate)	0	-	ns	

Note: *1 A valid data delay on HDAT is admitted 12ns from assert of HACK.

Table 9-8-2 AC characteristics-Host Bus DMA mode (the decompression controlled by HACK and PACK)

9.9 Pixel Bus DMA mode (write)

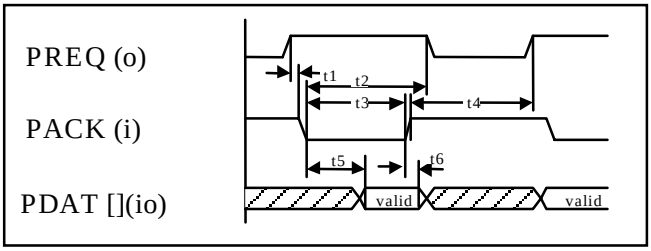


Figure 9-9-1 Pixel Bus DMA write timing

Symbol	Parameter	Min	Max	Unit	Conditions
t1	PREQ Assert - PACK Assert	0	-	ns	
t2	PACK Assert - PREQ Negate	0.5T	2.5T	ns	Output Loading is 50pF.
t3	PACK Assert Width	2T	-	ns	
t4	PACK Negate - PREQ Assert	2T	-	ns	Output Loading is 50pF.
t5	PDAT Setup Time (PACK Assert)	-12	-	ns	*1
t6	PDAT Hold Time (PACK Negate)	0	-	ns	

Note: *1 A valid data delay on PDAT is admitted 12ns from assert of PACK.

Table 9-9-2 AC characteristics-Pixel Bus DMA mode (write)

9.10 Pixel Bus DMA mode (read)

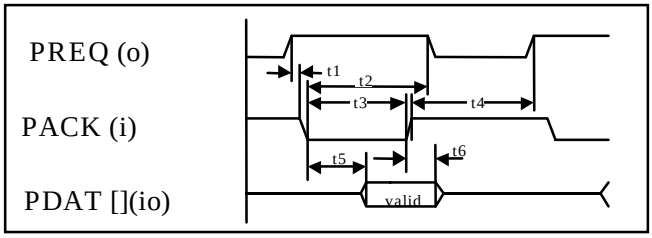


Figure 9-10-1 Pixel Bus DMA read timing

Symbol	Parameter	Min	Max	Unit	Conditions
t1	PREQ Assert - PACK Assert	0	-	ns	
t2	PACK Assert - PREQ Negate	0.5T	2.5T	ns	Output Loading is 50pF.
t3	PACK Assert Width	2T	-	ns	
t4	PACK Negate - PREQ Assert	2T	-	ns	Output Loading is 50pF.
t5	PACK Assert - PDAT Output Delay	-	18	ns	Output Loading is 50pF.
t6	PACK Negate - PDAT 3-state Delay	-	18	ns	Output Loading is 50pF.

Table 9-10-2 AC characteristics-Pixel Bus DMA mode (read)

9.11 Pixel Bus ・ Pixel Synchronous mode (write)

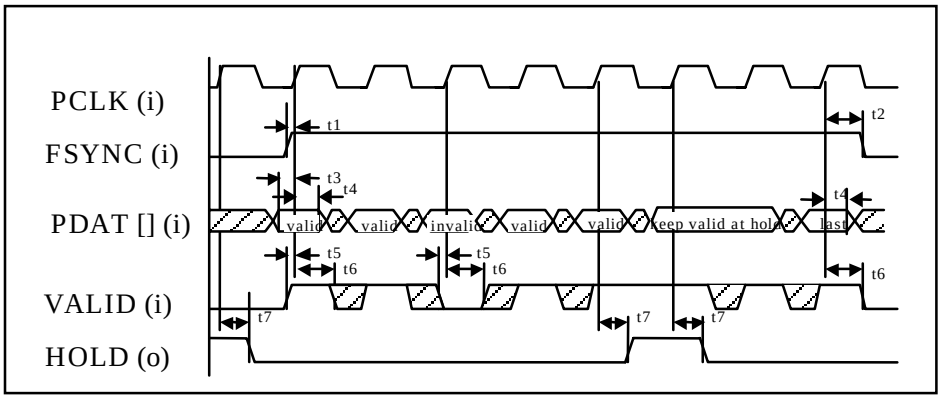


Figure 9-11-1 Pixel Bus Pixel Synchronous write timing

Symbol	Parameter	Min	Max	Unit	Conditions
t1	FSYNC Setup Time	8	-	ns	
t2	FSYNC Hold Time	3	-	ns	
t3	PDAT Setup Time	8	-	ns	
t4	PDAT Hold Time	3	-	ns	
t5	VALID Setup Time	8	-	ns	
t6	VALID Hold Time	3	-	ns	
t7	HOLD Output Delay	-	20	ns	Output Loading is 50pF.

Table 9-11-2 AC characteristics- Pixel Bus Pixel Synchronous mode (write)

9.12 Pixel Bus Pixel Synchronous mode (read)

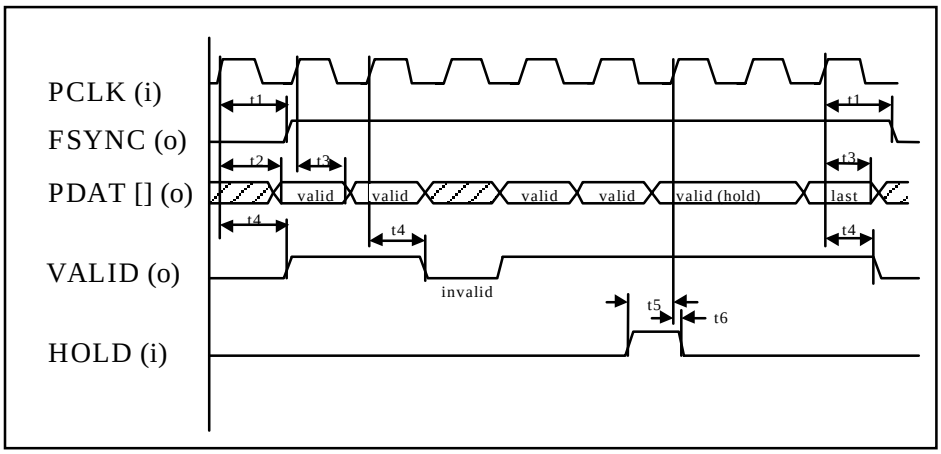


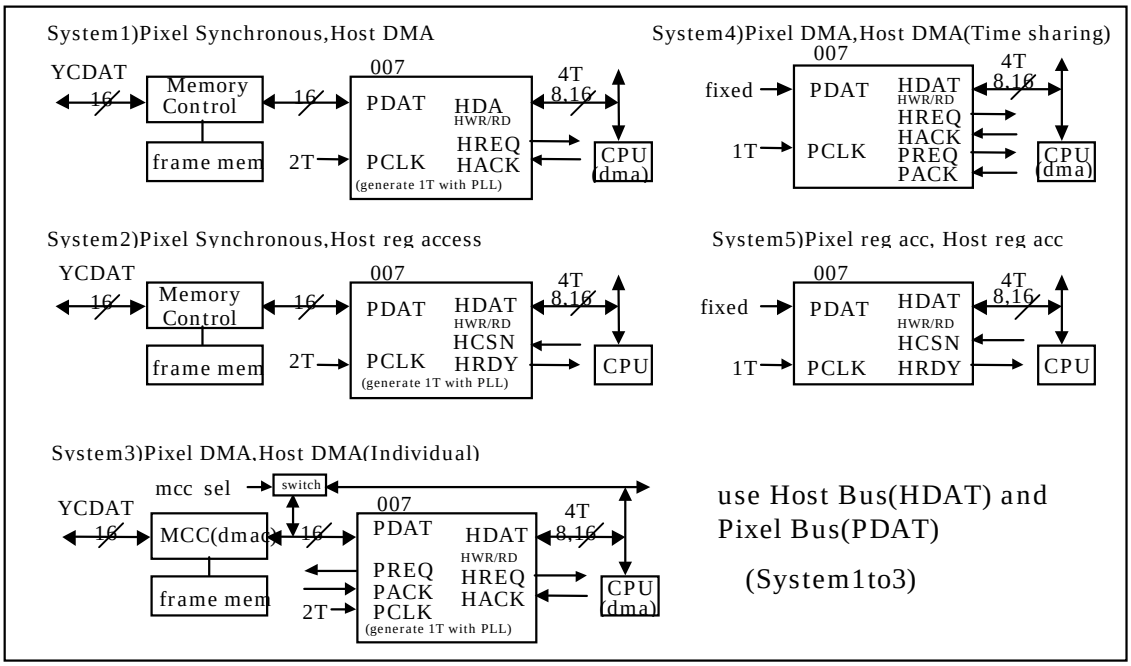
Figure 9-12-1 Pixel Bus Pixel Synchronous mode read timing

Symbol	Parameter	Min	Max	Unit	Conditions
t1	FSYNC Output Delay	-	20	ns	Output Loading is 50pF.
t2	PDAT Output Delay	-	20	ns	Output Loading is 50pF.
t3	PDAT Output Hold Time (PCLK Rise)	5	-	ns	Output Loading is 50pF.
t4	VALID Output Delay	-	20	ns	Output Loading is 50pF.
t5	HOLD Setup Time	8	-	ns	
t6	HOLD Hold Time	3	-	ns	

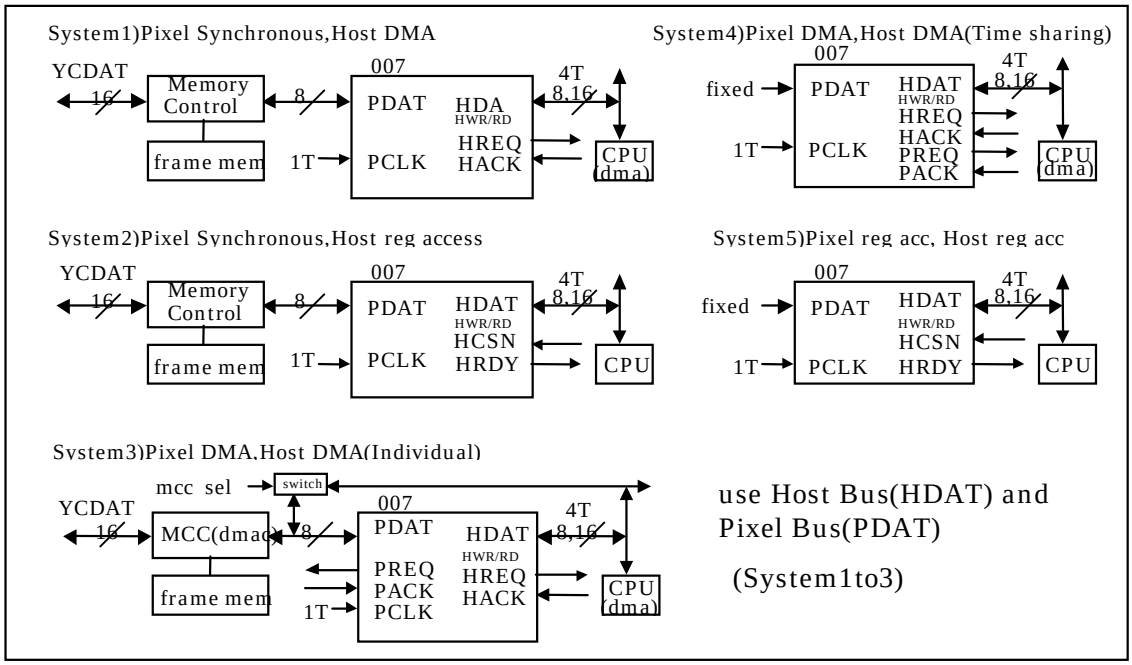
Table 9-12-2 AC characteristics- Pixel Bus Pixel Synchronous mode (read)

10) Typical System Configurations

Typical systems with LQFP-80 are shown as below.



Typical systems with LQFP-64 are shown as below. PCLK can be only 1T, because PLL is not available. In these systems, PIXEL BUS (PDAT) has only 8bits width.



11) Special differences between high speed JPEG chip (KL5A71007) and KL5A71006

No.	Parameter	KL5A71007	KL5A71006
1	Maximum Pixel Processing Rate	32Mbyte/sec	4Mbyte/sec
2	Maximum Frequency (Internal Clock)	32MHz	32MHz
3	Pixel Data In/Out at DMA mode	HOST BUS also usable	Only PIXEL BUS
4	Maximum Input Voltage	3.9V	5.5V
5	Package Types	L-QFP64(0.5mm) and LQP80(0.5mm)	LQFP80(0.5mm)
6	Supplying SYSCLK	x2 External CLK with PLL(80pins) or x1 External CLK	x1 External CLK
7	Encoding/Decoding RST Marker Code	Available at Comp and Decomp.	Only at Decomp
8	Register Access	Possible even at Comp/Decomp	Only when Flag is Asserted
9	No Data Output at Compression Process	Available	Not Available (need to read 1 word)
10	Polarity of REQ and ACK-pins	Programmable	REQ: Active High ACKN: Active Low
11	Register Mappings and Pin Assignments	New	-

12 64pin LQFP Package usage guide

12.1 Functionality restriction

LQFP-64 version has only 8 bits width Pixel Bus. Internal PLL is not usable on LQFP-64 version. Then there are restrictions as follows:

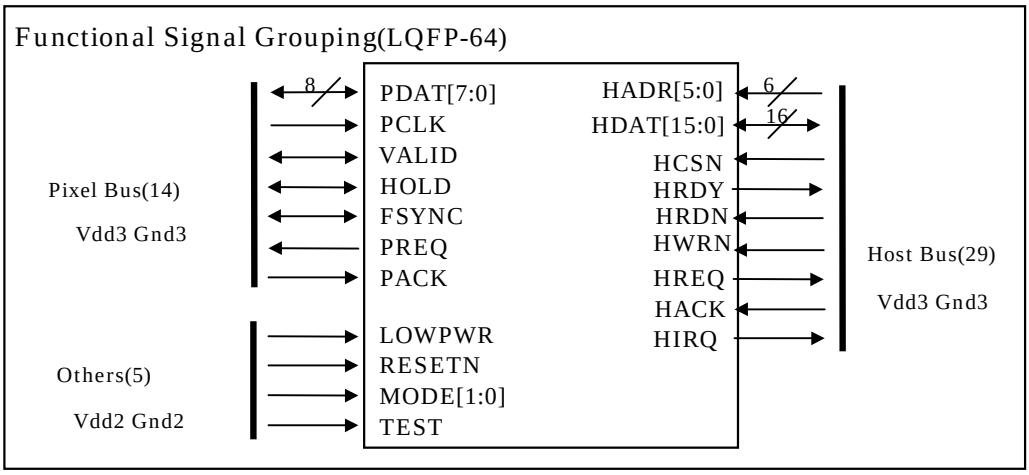
1) Pixel data must be in/out with 8bits width in the case of using Pixel Bus

In PCLK synchronous mode or PDMA individual mode, Pixel Bus has only 8 bits width for input/output. But if PDMA time sharing mode is selected, Pixel can be in/out with 16bits width on Host Bus.

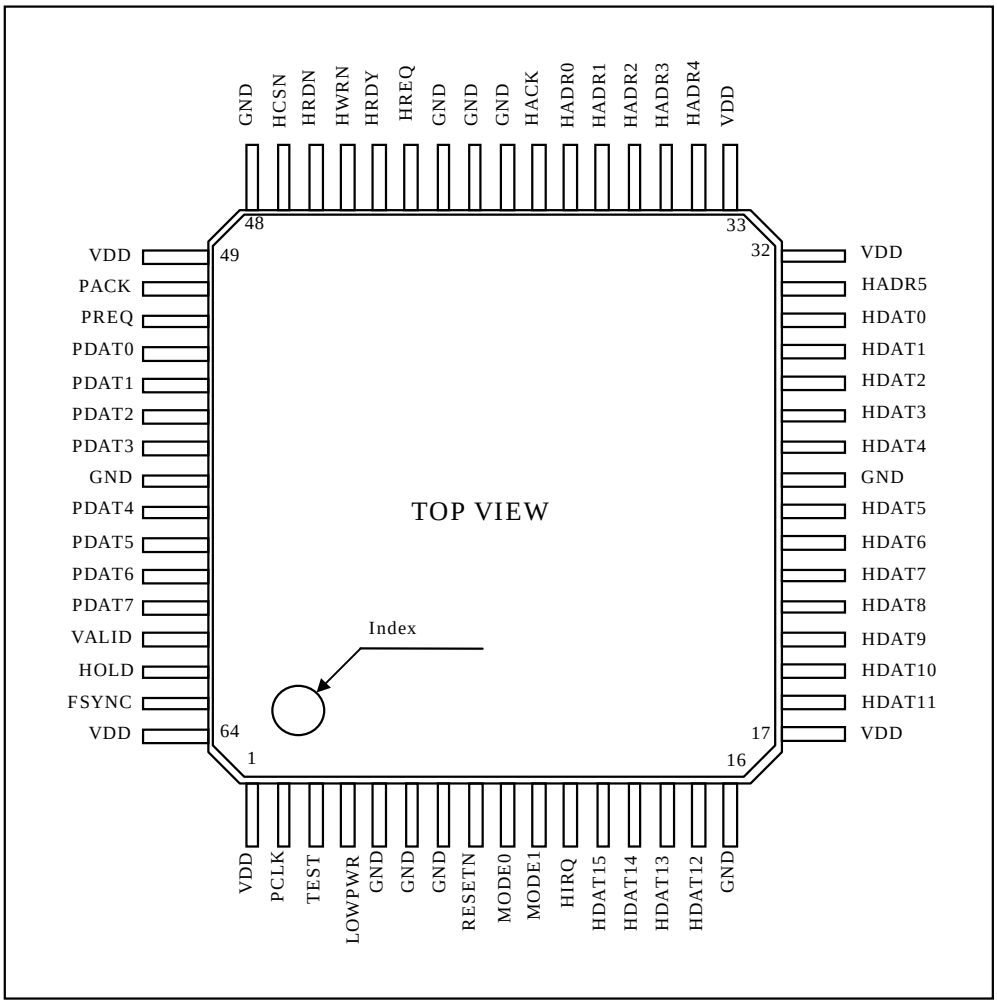
2) External CLK

The external CLK on PCLK-pin can be used as the internal CLK (SYSCLK).

12.2 64pin LQFP Layout



Pin Assignment（Top view）



12.3 Signal Description (LQFP-64)

No.	Pin name	Pin No.	I/O	Function
∗Host Bus interface				
1	HADR[5:0]	31, 34-38	I	This pin has the same function for LQFP-80. Please refer to “5) SIGNAL DESCRIPTIONS” for LQFP-80.
2	HDAT[15:0]	12-15, 18-24, 26-30	I/O	This pin has the same function for LQFP-80. Please refer to “5) SIGNAL DESCRIPTIONS” for LQFP-80.
3	HCSN	47	I	This pin has the same function for LQFP-80. Please refer to “5) SIGNAL DESCRIPTIONS” for LQFP-80.
4	HRDY	44	OT	This pin has the same function for LQFP-80. Please refer to “5) SIGNAL DESCRIPTIONS” for LQFP-80.
5	HRDN	46	I	This pin has the same function for LQFP-80. Please refer to “5) SIGNAL DESCRIPTIONS” for LQFP-80.
6	HWRN	45	I	This pin has the same function for LQFP-80. Please refer to “5) SIGNAL DESCRIPTIONS” for LQFP-80.
7	HREQ	43	O	This pin has the same function for LQFP-80. Please refer to “5) SIGNAL DESCRIPTIONS” for LQFP-80.
8	HACK	39	I	This pin has the same function for LQFP-80. Please refer to “5) SIGNAL DESCRIPTIONS” for LQFP-80.
9	HIRQ	11	O	This pin has the same function for LQFP-80. Please refer to “5) SIGNAL DESCRIPTIONS” for LQFP-80.
∗Pixel Bus interface				
10	PDAT[7:0]	60-57, 55-52	I/O	The PDAT[7:0] are “Pixel Data Bus” signals and for transferring pixel data in PCLK synchronous mode and individual DMA mode. In time sharing DMA mode and register access mode, please connect PDAT to H or L. The LSB is PDAT[0].
11	PCLK	2	I	This pin has the same function for LQFP-80. Please refer to “5) SIGNAL DESCRIPTIONS” for LQFP-80.
12	VALID	61	I/O	This pin has the same function for LQFP-80. Please refer to “5) SIGNAL DESCRIPTIONS” for LQFP-80.
13	HOLD	62	I/O	This pin has the same function for LQFP-80. Please refer to “5) SIGNAL DESCRIPTIONS” for LQFP-80.
14	FSYNC	63	I/O	This pin has the same function for LQFP-80. Please refer to “5) SIGNAL DESCRIPTIONS” for LQFP-80.

12.3 Signal Descriptions (LQFP-64)

No.	Pin name	Pin No.	I/O	Function
*Pixel Bus				
15	PREQ	51	O	This pin has the same function for LQFP-80. Please refer to “5) SIGNAL DESCRIPTIONS” for LQFP-80.
16	PACK	50	I	This pin has the same function for LQFP-80. Please refer to “5) SIGNAL DESCRIPTIONS” for LQFP-80.
*Others				
17	LOWPWR	4	I	This pin has the same function for LQFP-80. Please refer to “5) SIGNAL DESCRIPTIONS” for LQFP-80.
18	RESETN	8	I	This pin has the same function for LQFP-80. Please refer to “5) SIGNAL DESCRIPTIONS” for LQFP-80.
19	TEST	3	I	The TEST is “Test Mode Control Signal”. Please connect to GND.
20	MODE[1:0]	10,9	I	The MODE[1:0] are “Chip Mode Control” signals. Please hold MODE[1:0] to b00.

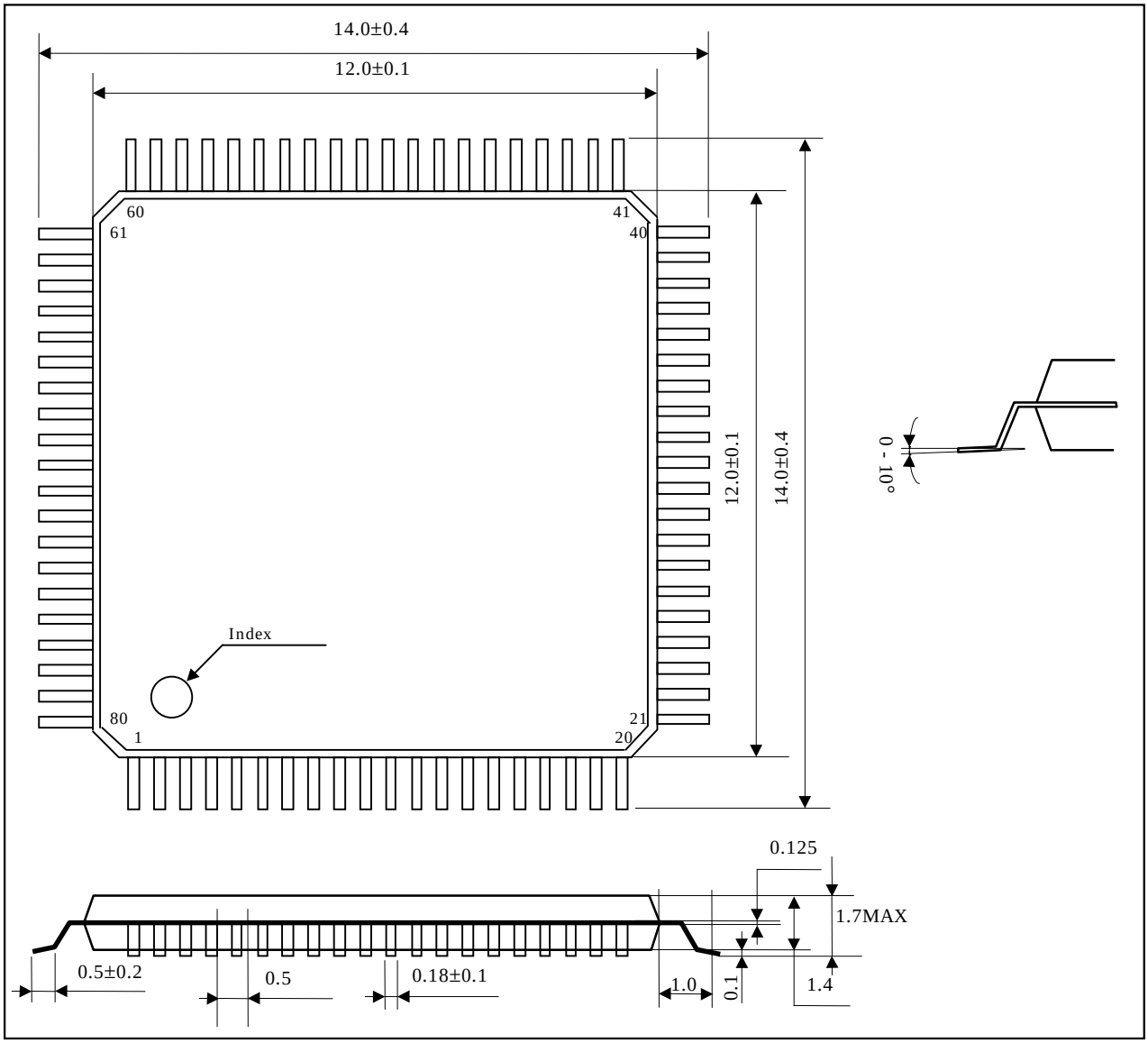
13) Package Specification

Package data and diagrams for LQFP-80 and LQFP-64 are shown as follows.

Figure 13-1 LQFP-80 Package data

No.	Parameter	Value	Unit
1	Lead Pitch	0.5	mm
2	Package Body	12.0 (typical)	mm
3	Terminal Dimension	14.0 (typical)	mm
4	Package Height	1.6 (max)	mm

Fig. 13-2 LQFP-80 Package diagram

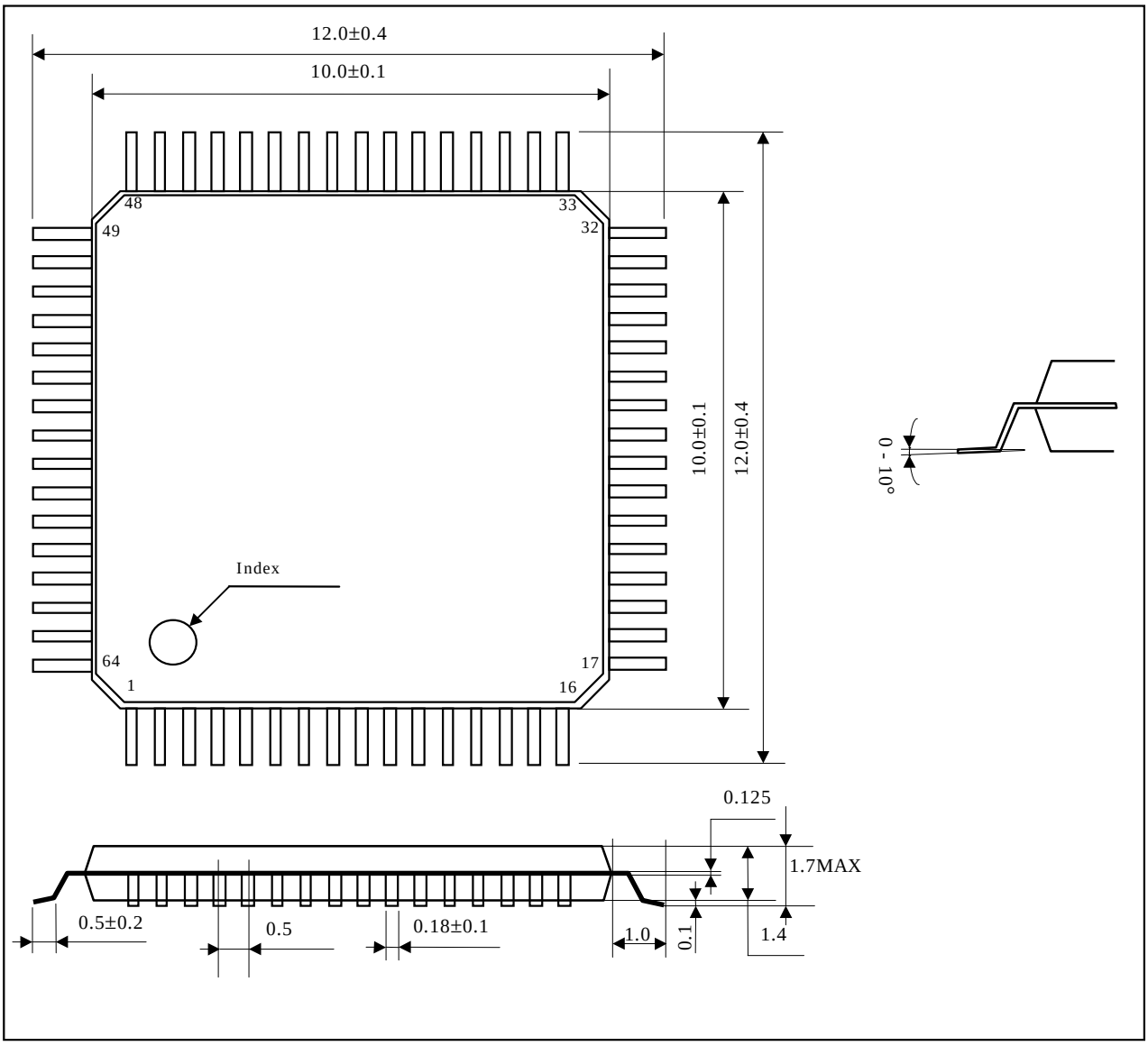


13) Package Specification

Fig. 13-3 LQFP-64 Package data

No.	Parameter	Value	Unit
1	Lead Pitch	0.5	mm
2	Package Body	10.0 (typical)	mm
3	Terminal Dimension	12.0 (typical)	mm
4	Package Height	1.7 (max)	mm

Fig. 13-4 LQFP-64 Package diagram



14) Known Bug list

14.1 restriction of Huffman table in compression

14.1.1 conditions

In compression, there is 1 bit length Huffman table.

14.1.2 action

KL5A71007 can not compress normally.

14.1.3 comment

If Huffman tables described in ISO/IEC 10918-1 are used, there are no problems. In decompression, this problem does not occur.

14.2 restriction of Huffman table in decompression

14.2.1 conditions

In decompression, the number of HUFFVAL list is shorter than 12 in DC or 162 in AC.

14.2.2 action

KL5A71007 can not decode DHT.

14.2.3 comment

If the number of HUFFVAL list is shorter than 12 in DC or 162 in AC, please add the dummy HUFFVALs, for instance h00, at the end of each HUFFVAL to arrange the number of list, and change Lh parameter to proper value. After that, KL5A71007 can decompress normally.

14.3 restriction in set up Table data

14.3.1 condition

During setting up the Table data, change the address and assert the HWRN or HRDN before end of writing whole table data.

14.3.2 action

Table data will not be set up correctly and stop the operation.

14.3.3 comment

While set up the table data, write the table data continuously that start with the DQT or DHT, and never change the address.

14.4 restriction in DMA de-compression

14.4.1 condition

While DMA mode de-compression, assert HWRN or HRDN with setting the address h10 or h2C.

14.4.2 action

The de-compression process will not complete correctly.

14.4.3 comment

While DMA mode de-compression, use this chip without HWRN or HRDN or never set the address h10 or h2C.

15) Glossary

Block:
An 8x8 array of data samples

Coefficient:
The amplitude of a specific cosine basis function in a discrete cosine transform. Also called DCT coefficient. A DC coefficient is the coefficient for which the frequency is zero in both dimensions. An AC coefficient is one for which the frequency is non-zero in at least one dimension.

Component:
A two-dimensional array of data samples. A component usually represents a single color. A set of components is an image.

Compression:
The process of reducing the number of bits required to represent an image.

Compression ratio:
The number of bits required to represent the source image divided by the number of bits required to represent the compressed image.

Discrete cosine transform(DCT):
A transform coding technique that uses cosine basis function to convert between a block and a corresponding array of basis-function amplitudes. A forward DCT(FDCT) converts from a block to an array of basis-function amplitudes; an inverse DCT(IDCT) converts from an array of basis-function amplitudes into a block.

Frame:
A two-dimensional subset of an image. All components in a frame have the same physical boundaries.

Huffman coding:
A lossless coding technique that assigns a variable-length code to each input value. In Huffman coding, frequently occurring patterns receive the shortest codes. Also called variable-length coding.

Image:
A single frame of intensity data that is a function of two spatial variables, x and y. An image is made up of one or more components that contain the data from which a visual display can be reconstructed. A color image contains more than one component; a grayscale image contains a single component. A compressed image is a coded representation of an image as specified by JPEG-9-R6. A source image is the input to an encoder. A reconstructed

image is an image that has been created by a decoder.

Interleaved:
The repetitive multiplexing of small groups of blocks from each components in a specific order. Also called block interleaved.

Minimum coded unit:
The smallest grouping of data units that is coded. Data unit is the smallest recognized unit that can be processed by a coder. In DCT-based coding, a data unit is a block.

Quantization:
A process in which data is categorized into discrete values. By varying the quantization stepsize, the amount of information required to represent a signal can be reduced. Quantization is a lossy process.

Quantization stepsize:
The distance between possible values of the quantized signal.

Scanning order:
The ordering of data in the data units. In raster scanning, the data is ordered from left to right in rows, and the rows are ordered from top to bottom. In zigzag scanning, the data is ordered from upper left to lower right in a zigzag progression. In blocks of DCT coefficients, zigzag scanning arranges coefficients in ascending frequency, increasing the efficiency of the run-length coding.

16) Index

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