Motion JPEG Chip KL5A72002 datasheet

Rev 0.8

Preliminary

Kawasaki Steel Corporation
LSI division

1. Revision history

Rev.	date	The contents of updating
0.1	98.12.17	First release
0.8	99.12.20	Release as KL5A72002

2. Notes

This document is preliminary version and may be changed without notice.

Kawasaki Steel Corporation reserves the right to make changes to the specifications herein at any time without notice.

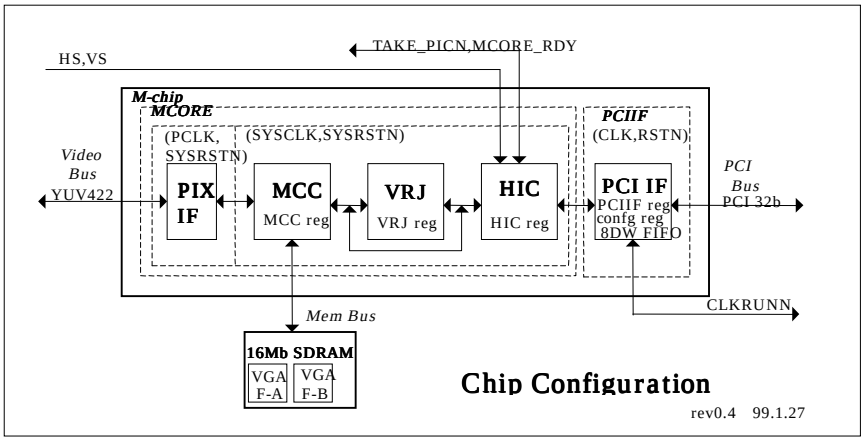
Kawasaki Steel Corporation does not assume any responsibility or liability arising out of the application or use of any circuit or information described herein; neither does it convey any license under its patent rights, intellectual property rights, or any other rights of Kawasaki Steel Corporation or of third parties.

Please refer to each datasheet for detail information about JPEG and SDRAM.

3. Content

4. functional specification 4
5. pin and signal information 10
6. package pin asignment (6A: FBGA176, 6B: LQFP176) 11,13
7. package pin list (7A: FBGA176, 7B: LQFP176) 12,14
8. pin specification 15
9. state transition diagram 21
10. operation timing outline 24
11. evaluation board 25
12. memory map 26
12.1 PCI configuration space 27
12.2 Memory Mapping space (MCORE register) 33
12.3 Frame Memory map 45
12.4 Main Memory Access Method (PCI Master Operation of Continuation Processing) 47
13. device control flow 49
14. example of initial setting 50
15. electric specification 53
16. package outline 63
17. known bug 65

4. Functional specification



PIX IF : pixel data interface

MCC : SDRAM controller

VRJ : high speed JPEG (KL5A71007)

HIC : host interface, chip controller

PCI IF : PCI interface

4.1 Through image display (only in digital YC mode)

- Register setting to external digital video codec and YCDATA transfer from Decoder to Encoder

4.2 Frame memory control

- Initial setting to frame memory (SDRAM 1M x 16b), set refresh and lowpower
- Target SDRAM is KM416S1120, 512K X 16Bit X 2 Banks 100MHz or Equivalent Article
- Perform auto refresh 5 times / 1H synchronizing with rising edge of HS
- When the pulse interval of HS becomes more than 66µsec, refreshment timing is automatically calculated inside and refreshment of SDRAM is continued at 5 times every 66 µsec.
- When LSI is set as the low power mode, a power down setup is performed to SDRAM and it is set as the low power-consumption mode. The data of SDRAM are lost at this time.

4.3 Frame memory access

- Direct writing and read out to/from SDRAM
- Access SDRAM through the register of MCC block in PCI target mode.
- Possible to access linear and continuously from set-up initial address to Memory Space.
- 1024 pixel x 1024 line(max), YUV=422 image is stored in frame memory
- In motion processing mode, 2 VGA size image is processed alternatively

4.4 Still image capture

- Capture 1 frame still image(YUV=422)
- Selectable 2 mode video bus interface

ZV-port mode : YUV=422, progressive VGA image input
YC[15:0], HS, VS, PCLK

Digital YC mode : YUV=422 interlace VGA image input
YC, HS, VS, PCLK, ODD, DOE

- Capture position and range is set to register as H_(V_)START and H_(V_)COUNT.
- 1/2 sub-sampling both horizontal and vertical is possible during image capture.
- The execution timing of a command synchronizes with VS which shows frame start.

4.5 Display (only in digital YC mode)

- Display image stored in frame memory
- Displayed image area is set to register, R_X(Y)BASE and R_X(Y)RANGE
- Continue display untill the stop display command (NO DISP) is execute
- The execution timing of a command synchronizes with VS of the first field.

4.6 JPEG Independent Compression

- Pixel data of block interleave format is written to the chip in PCI target mode and compressed with an internal JPEG core and JPEG compression data is output in PCI target mode, time shared with pixel data.

4.7 JPEG Independent de-compression

- JPEG compression data is written to the chip in PCI target mode, de-compressed with an internal JPEG core, and block inter-leave picture data is output in PCI target mode.

4.8 Still Image Compression

- 1 frame image compression stored in frame memory and data output in PCI target or master mode.
- The memory storing range of target picture data can be specified by register setup by B_X(Y) BASE and B_X(Y) RANGE.
- A command is executed immediately, without synchronizing with VS.

4.9 Still Image Output

- One Frame Read-out, data output in PCI Target or Master mode of Frame Memory Storing Picture.
- The memory storing range of target picture data can be specified by register setup by B_X(Y) BASE and B_X(Y) RANGE.
- A command is executed immediately, without synchronizing with VS.

4.10 Still Image De-Compression

- 1 Frame compressed data input in PCI Target or master mode, de-compress and data store to frame memory.

- The memory storing range of target picture data can be specified by register setup by B_X(Y) BASE and B_X(Y) RANGE.

- A command is executed immediately, without synchronizing with VS.

4.11 Still Image Capture and Compression

- 1 frame still image capture, compression and data output in PCI target or master mode.

- It can perform by combining two micro commands, still picture capture processing of 4.4, and still picture compression processing of 4.8.

4.12 Still image De-compression & Display (only in digital YC mode)

- 1 frame compressed data input in PCI target or master mode and de-compress, store to frame memory

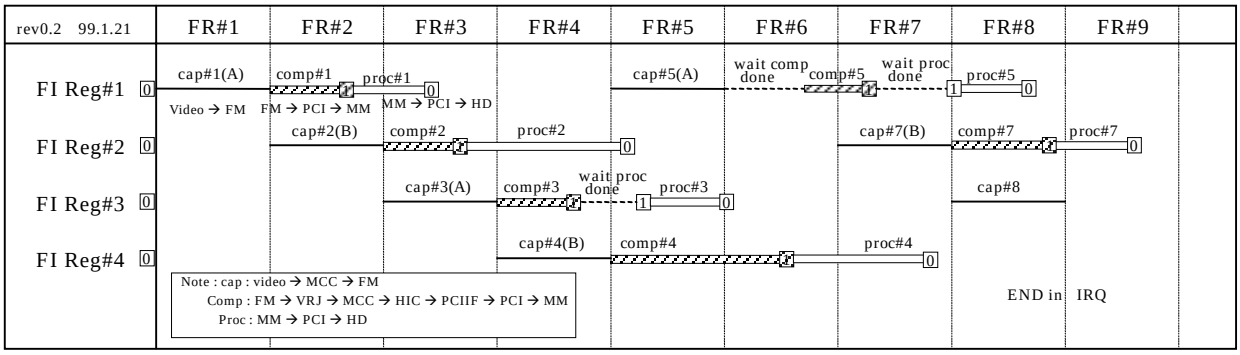
- It can perform by combining two micro commands, still picture de-compression of 4.9, and still picture display of 4.5.

4.13 Continuous Picture Capture & Compression

- Capture and compression every N frame, data output to main memory in PCI master mode

- Frame interval N is set to register, the value is from 0 (every frame) to 31 (every 32 frames)

- When a bottleneck is in a processing flow and processing is not completed within the specified frame time, the subsequent frame picture for processing is missing.



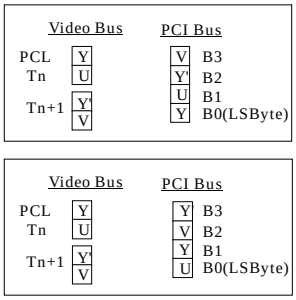
4.14 Continuous Picture Output

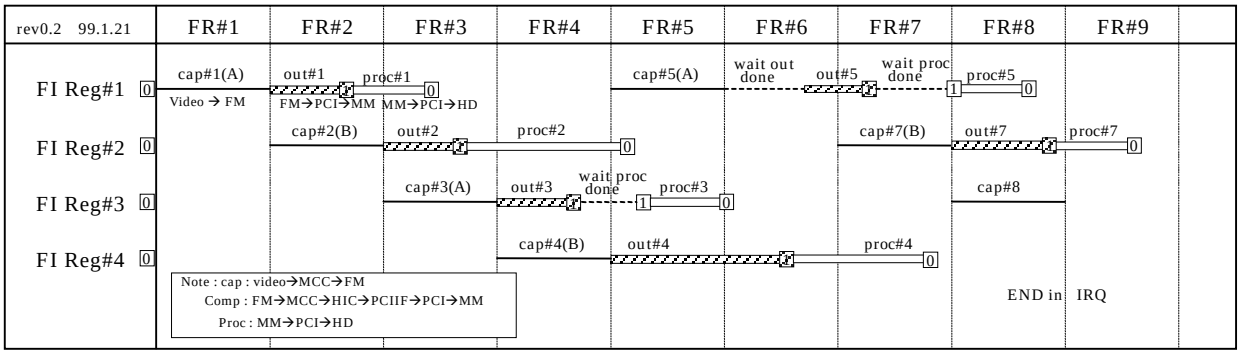
- Every N frame capture, frame memory read-out and data output to main memory in PCI master mode

- Frame interval N is set to register, the value is from 0 (every frame) to 31 (every 32 frames)

- When a bottleneck is in a processing flow and processing is not completed within the specified frame time, the subsequent frame picture for processing is missing.

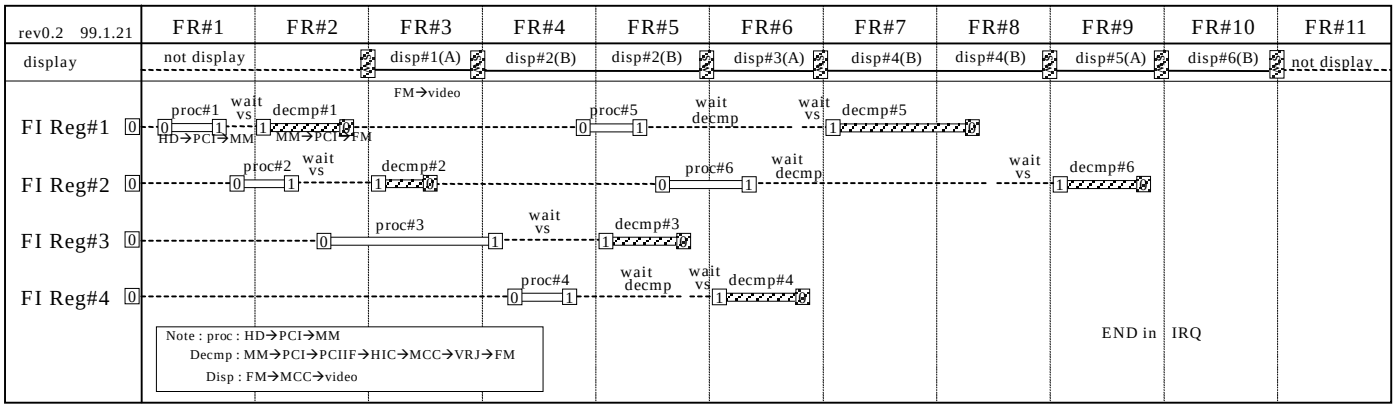
- The picture output format to a PCI bus is pixel sequential and the byte arrangement is as follows





4.15 Continuous Picture de-compression & Display (only in digital YC mode)

- Read-out from main memory in PCI master mode and de-compression, store to frame memory and display. Display changes when a frame memory is updated (every N frames).
- Frame interval N is set to register, the value is from 0 (every frame) to 31 (every 32 frames)
- When a bottleneck is in a processing flow and processing is not completed within the specified frame time, the subsequent frame picture for processing is missing.



4.16 Camera Capture

- If a TAKE_PICN signal is made active when an internal flag HOST_USEREQ is 0, the VGA size still image will be captured in the next VS term.
- When the picture captured by camera capture processing is in a frame memory, an internal PIC_SAVED flag is set.
- A past capture data is overwritten when two or more TAKE_PICN signal pulse inputs.
- An internal TP_BUSY flag is set to 1 during camera capture processing execution.
- When a TP_BUSY flag is 0 and a HOST_USEREQ flag is 1, a TAKE_PICN pulse input is disregarded.

4.17 Low Power Mode

- If LOWPOWER register in HIC register domain is set to 1, this chip will set the SDRAM to power down mode, and will suspend the clock inside MCORE.
- When LOWPOWER register is set, negate a MCORE_RDY signal.
- Setup and release of LOWPOWER register must be performed when HOST_USEREQ is 1.

Note: Even when HOST_USEREQ is 0, a setup and release are possible for LOWPOWER register.
However, if LSI is not idle, incorrect operation may be performed after release.
In this case, it is required to input a soft reset command and to initialize a chip.
(This means canceling lowpower mode with a soft reset flag.)

- A setup, release, and a monitor of LOWPOWER register are possible by PCI configuration access. A setup and release of LOWPOWER should be based on the setup and release by LOWPOWER register.

4.18 PCI CLKRUNN signal

- When device status is in D0 (ACTIVE) and a HOST_USEREQ flag is 1, this chip requires that PCI CLK is 33MHz. When CLKRUNN is negated and change of clock speed is notified, a device asserts 1T term of the CLKRUNN, and requires hold a clock to 33MHz.

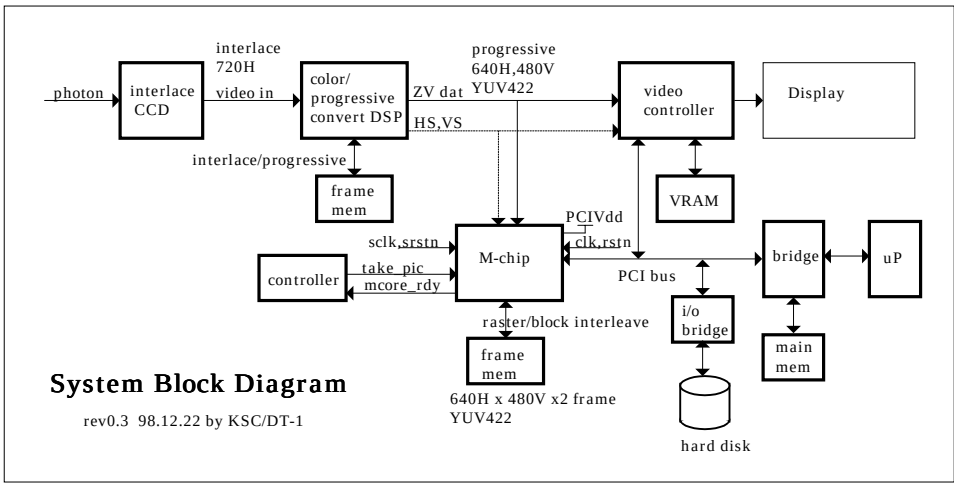
Note : It is not concerned with device status in fact, but when a HOST_USEREQ flag is 1, it is always required that PCI CLK is 33MHz.

4.19 Reset of MCORE block

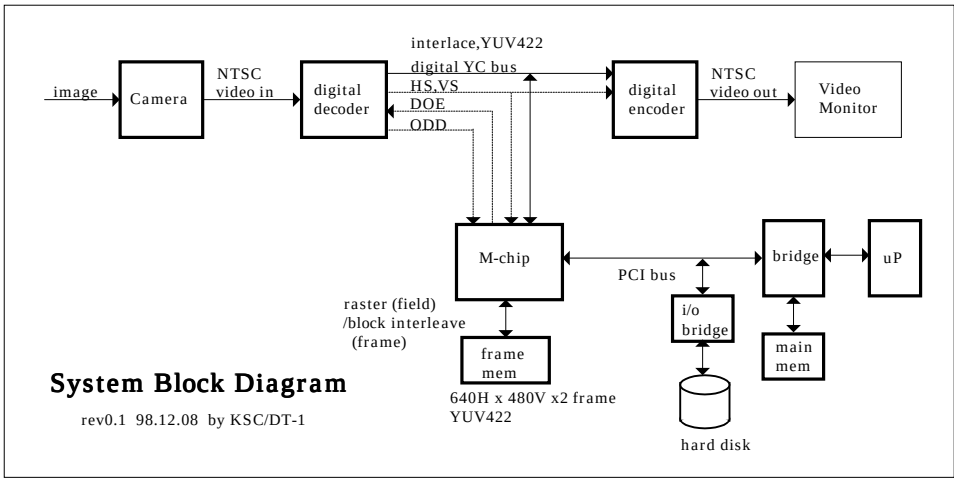
- Initialization inside MCORE block is performed by the assert of SYSRSTN, or the soft reset flag. Initialization of SDRAM is performed after an end of reset.

4.20 Example of system configuration

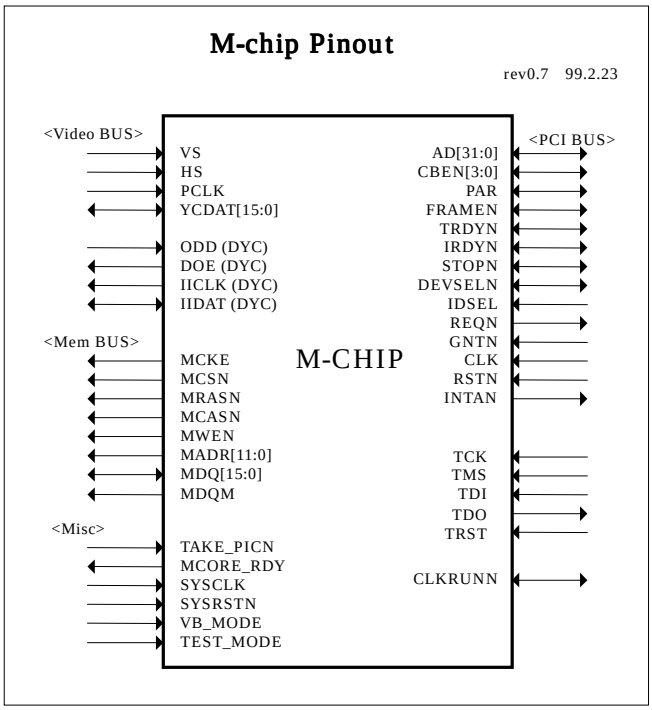
* ZV-port mode :



* Digital YC mode :



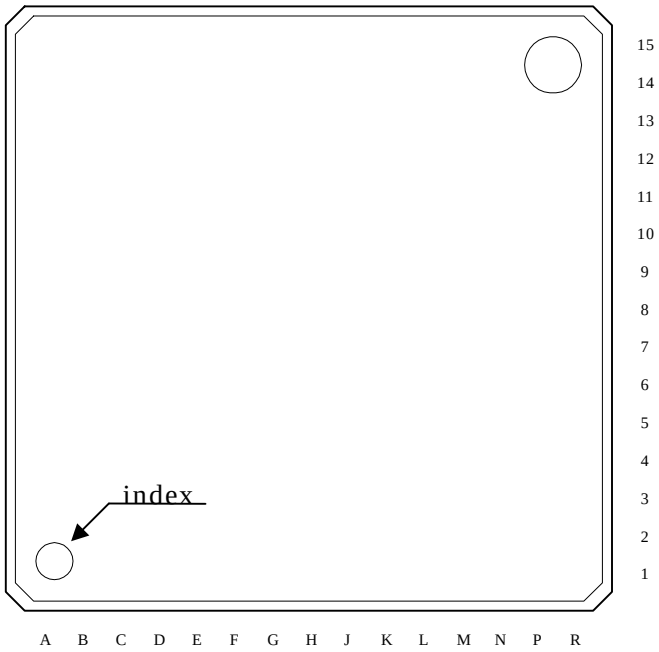
5. Logical signal arrangement



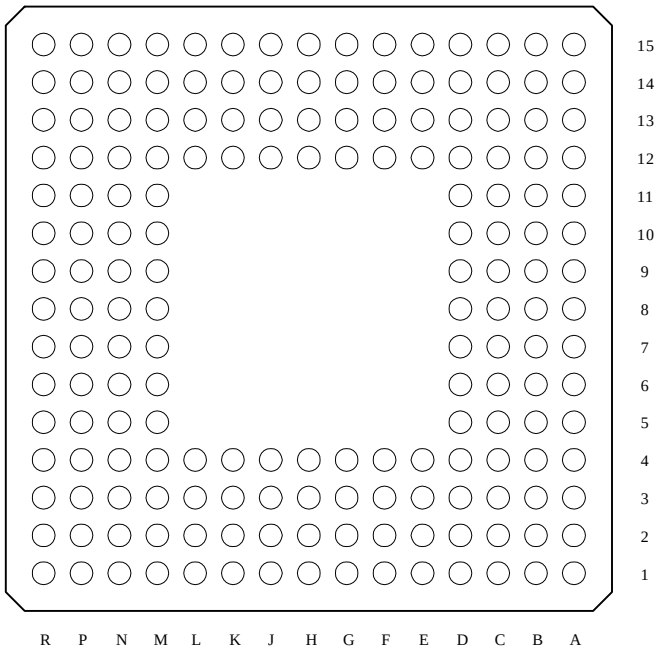
6A. Pin arranegement diagram (FBGA176)

The pin arrangement of FBGA176 package is shown below.

TOP VIEW



BOTTOM



7A. Package pin table (FBGA176)

The pin of FBGA176 package and correspondence of a signal name are shown below.

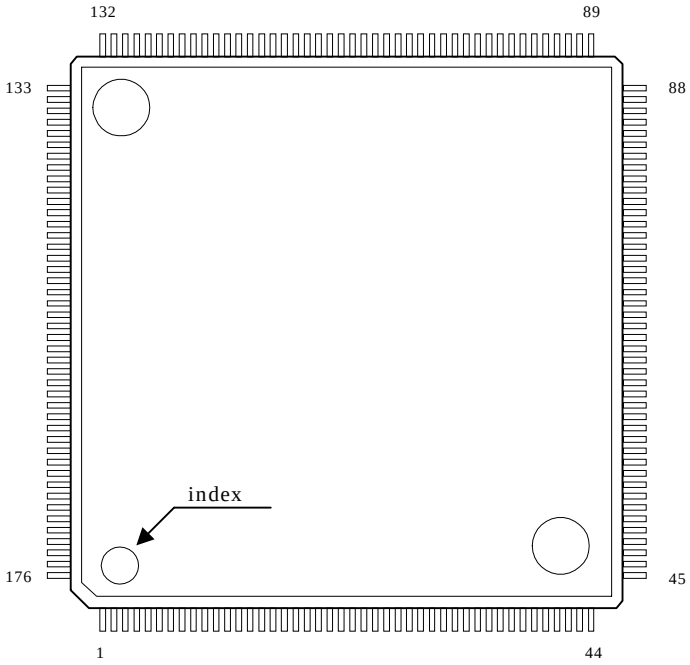
FBGA176 pin table rev 0.4 99.2.12

Pin No.	I/O	Signal name	Pin No.	I/O	Signal name	Pin No.	I/O	Signal name	Pin No.	I/O	Signal name
A1	I/O	AD30	C15	I/O	MDAT2	H12	I/O	MDAT11	N2	I/O	AD14
A2	-	gnd	D1	-	gnd	H13	-	gnd	N3	-	vdd
A3	I	GNTN	D2	I/O	AD25	H14	-	gnd	N4	I/O	AD10
A4	O	INTAN	D3	I/O	AD28	H15	-	gnd	N5	-	vdd
A5	I	TDI (JTAG)	D4	I/O	AD29	J1	I/O	AD16	N6	I/O	AD6
A6	I	TRST (JTAG)	D5	I/O	CLKRUNN	J2	-	vdd	N7	I/O	AD4
A7	I	HS	D6	I	TMS (JTAG)	J3	-	gnd	N8	I/O	AD1
A8	-	vdd	D7	I	ODD	J4	I/O	AD17	N9	O	MDQM
A9	I/O	YCDAT12	D8	I/O	YCDAT9	J12	I/O	MDAT14	N10	-	gnd
A10	I/O	YCDAT15	D9	I/O	YCDAT11	J13	I/O	MDAT13	N11	-	vdd
A11	I/O	YCDAT0	D10	-	vdd	J14	I/O	MDAT12	N12	-	vdd
A12	I/O	YCDAT3	D11	I/O	YCDAT2	J15	-	vdd	N13	-	vdd
A13	-	vdd	D12	I/O	YCDAT7	K1	I/O	FRAMEN	N14	O	MADR3
A14	I/O	YCDAT6	D13	-	vdd	K2	-	gnd	N15	O	MADR0
A15	I/O	IIDAT	D14	-	gnd	K3	I/O	IRDYN	P1	I/O	CBEN1
B1	-	gnd	D15	-	vdd	K4	I/O	CBEN2	P2	-	gnd
B2	-	gnd	E1	I/O	CBEN3	K12	-	vdd	P3	I/O	AD11
B3	I/O	AD31	E2	I	IDSEL	K13	-	gnd	P4	-	gnd
B4	O	REQN	E3	I/O	AD24	K14	O	MCKE	P5	I/O	CBEN0
B5	I	CLK	E4	-	vdd	K15	I/O	MDAT15	P6	-	gnd
B6	-	gnd	E12	I/O	MDAT4	L1	I/O	TRDYN	P7	I/O	AD2
B7	I	TCK (JTAG)	E13	I/O	MDAT3	L2	I/O	STOPN	P8	-	gnd
B8	I	VS	E14	I/O	MDAT0	L3	-	gnd	P9	I	TEST_MODE
B9	I/O	YCDAT10	E15	I/O	MDAT6	L4	I/O	DEVSELN	P10	I	TAKE_PICN
B10	I/O	YCDAT13	F1	I/O	AD22	L12	-	gnd	P11	O	MADR10
B11	-	gnd	F2	I/O	AD21	L13	O	MWEN	P12	-	gnd
B12	I/O	YCDAT4	F3	-	gnd	L14	O	MRASN	P13	O	MADR7
B13	I/O	YCDAT5	F4	I/O	AD23	L15	O	MCSN	P14	O	MADR4
B14	I	PCLK	F12	I/O	MDAT7	M1	-	vdd	P15	O	MADR1
B15	I/O	MDAT1	F13	I/O	MDAT5	M2	-	gnd	R1	I/O	AD12
C1	I/O	AD26	F14	-	gnd	M3	-	vdd	R2	-	gnd
C2	I/O	AD27	F15	-	vdd	M4	I/O	AD15	R3	I/O	AD9
C3	-	vdd	G1	I/O	AD20	M5	I/O	AD13	R4	I/O	AD8
C4	-	vdd	G2	I/O	AD19	M6	-	gnd	R5	I/O	AD7
C5	I	RSTN	G3	-	vdd	M7	-	vdd	R6	I/O	AD5
C6	O	TDO (JTAG)	G4	-	gnd	M8	-	gnd	R7	I/O	AD3
C7	O	DOE	G12	I/O	MDAT9	M9	-	vdd	R8	I/O	AD0
C8	I/O	YCDAT8	G13	-	gnd	M10	-	gnd	R9	I	VB_MODE
C9	-	gnd	G14	I/O	MDAT8	M11	O	MCORE_RDY	R10	I	SYSCLK
C10	I/O	YCDAT14	G15	I/O	MDAT10	M12	O	MADR5	R11	I	SYSRSTN
C11	I/O	YCDAT1	H1	-	gnd	M13	O	MADR2	R12	O	MADR11
C12	-	gnd	H2	-	gnd	M14	-	gnd	R13	O	MADR9
C13	-	vdd	H3	-	gnd	M15	O	MCASN	R14	O	MADR8
C14	O	IICLK	H4	I/O	AD18	N1	I/O	PAR	R15	O	MADR6

6B. Pin arranegement diagram (LQFP176)

The pin arrangement of LQFP176 package is shown below.

TOP VIEW



7B. Package pin table (LQFP176)

The pin of LQFP176 package and correspondence of a signal name are shown below.

LQFP176 pin table rev 0.3 99.2.12

Pin No.	I/O	Signal name	Pin No.	I/O	Signal name	Pin No.	I/O	Signal name	Pin No.	I/O	Signal name
1	-	vdd	45	-	vdd	89	-	vdd	133	-	vdd
2	I/O	AD29	46	I/O	AD13	90	O	MADR4	134	I/O	YCDAT7
3	I/O	AD28	47	I/O	AD12	91	O	MADR3	135	I/O	YCDAT6
4	I/O	AD27	48	I/O	AD11	92	-	gnd	136	I/O	YCDAT5
5	-	gnd	49	-	gnd	93	O	MADR2	137	-	vdd
6	I/O	AD26	50	I/O	AD10	94	O	MADR1	138	-	gnd
7	I/O	AD25	51	I/O	AD9	95	O	MADR0	139	I/O	YCDAT4
8	-	gnd	52	-	gnd	96	-	gnd	140	I/O	YCDAT3
9	-	vdd	53	-	vdd	97	O	MWEN	141	I/O	YCDAT2
10	I/O	AD24	54	I/O	AD8	98	O	MCASN	142	I/O	YCDAT1
11	I/O	CBEN3	55	I/O	CBEN0	99	O	MRASN	143	I/O	YCDAT0
12	I	IDSEL	56	I/O	AD7	100	-	vdd	144	-	gnd
13	I/O	AD23	57	-	gnd	101	O	MCSN	145	-	vdd
14	-	gnd	58	I/O	AD6	102	-	gnd	146	I/O	YCDAT15
15	I/O	AD22	59	I/O	AD5	103	O	MCKE	147	I/O	YCDAT14
16	I/O	AD21	60	-	gnd	104	I/O	MDAT15	148	I/O	YCDAT13
17	-	gnd	61	-	vdd	105	I/O	MDAT14	149	I/O	YCDAT12
18	-	vdd	62	I/O	AD4	106	I/O	MDAT13	150	I/O	YCDAT11
19	I/O	AD20	63	I/O	AD3	107	-	vdd	151	-	gnd
20	I/O	AD19	64	I/O	AD2	108	I/O	MDAT12	152	-	vdd
21	-	gnd	65	-	gnd	109	I/O	MDAT11	153	I/O	YCDAT10
22	-	gnd	66	I/O	AD1	110	-	gnd	154	I/O	YCDAT9
23	-	gnd	67	I/O	AD0	111	-	gnd	155	I/O	YCDAT8
24	I/O	AD18	68	-	gnd	112	-	gnd	156	I	HS
25	I/O	AD17	69	-	vdd	113	I/O	MDAT10	157	I	VS
26	I/O	AD16	70	O	MDQM	114	I/O	MDAT9	158	I	ODD
27	-	gnd	71	I	VB_MODE	115	-	gnd	159	O	DOE
28	-	vdd	72	I	TEST_MODE	116	-	vdd	160	I	TRST (JTAG)
29	I/O	CBEN2	73	-	gnd	117	I/O	MDAT8	161	I	TCK (JTAG)
30	I/O	FRAMEN	74	I	SYSCLK	118	I/O	MDAT7	162	I	TMS (JTAG)
31	I/O	IRDYN	75	-	gnd	119	I/O	MDAT6	163	O	TDO (JTAG)
32	-	gnd	76	I	SYSRSTN	120	I/O	MDAT5	164	I	TDI (JTAG)
33	I/O	TRDYN	77	I	TAKE_PICN	121	-	gnd	165	-	gnd
34	I/O	DEVSELN	78	O	MCORE_RDY	122	-	vdd	166	I/O	CLKRUNN
35	-	gnd	79	O	MADR11	123	I/O	MDAT4	167	O	INTAN
36	-	vdd	80	O	MADR10	124	I/O	MDAT3	168	I	RSTN
37	I/O	STOPN	81	O	MADR9	125	I/O	MDAT2	169	I	CLK
38	I/O	PAR	82	O	MADR8	126	I/O	MDAT1	170	I	GNTN
39	I/O	CBEN1	83	-	gnd	127	-	gnd	171	O	REQN
40	-	gnd	84	-	vdd	128	I/O	MDAT0	172	-	gnd
41	I/O	AD15	85	O	MADR7	129	I/O	IIDAT	173	I/O	AD31
42	I/O	AD14	86	O	MADR6	130	O	IICLK	174	I/O	AD30
43	-	gnd	87	O	MADR5	131	I	PCLK	175	-	gnd
44	-	vdd	88	-	vdd	132	-	vdd	176	-	vdd

8. Signal specification

No.	Signal name	I/O	Function
1	**PCI Bus**		
1-1	AD[31:0] (t/s)	I/O	PCI address, data bus. The cycle which asserted FRAMEN is an address phase. In a data phase, when it asserts IRDYN and TRDYN simultaneously, data transmission is performed. Endian form is Little Endian form that Most Significant Byte are stored in AD [31:24] (high byte address) and Least Significant Byte in AD [7:0] (low byte address).
1-2	CBEN[3:0] (t/s)	I/O	Bus command, byte enable signal. This signal expresses a command in an address phase, and expresses a byte enable in a data phase. In master operation, it becomes an output and input in an target operation. With this product, data transmission is always performed by DWORD (32b), it always outputs CBEN=0h at the time of master operation, in CBEN=Fh, repeals data transmission at the time of target operation (NULL data phase), and otherwise performs transmission processing as data of DWORD. Byte access by CBEN is supported at the time of a configuration.
1-3	PAR (t/s)	I/O	Even Parity flag. PAR is set up so that the sum total of the number of bits 1 of AD [31:0], CBEN [3:0], and PAR may serve as even number. PAR is outputted by 1T delay at the time of AD output, parity is calculated at the time of AD input, and it compares with PAR input value. The status register [15] of Config space is set to 1 at the time of data parity error detection. The status register [15] of Config space is set to 1 at the time of address parity error detection and when the command register [8, 6] is set, a status register [14] is set to 1.
1-4	FRAMEN (s/t/s)	I/O	Cycle frame signal. Outputs at the time of master operation. It is shown that it is among bus transmission start and a cycle. It becomes TS output in master mode and becomes an input in target mode.
1-5	TRDYN (s/t/s)	I/O	Target RDY signal. It is shown that the data transmission preparation by the target side is ready. It becomes an input in master mode, and becomes TS output in target mode. It becomes possible only for DEVSELN assert term to output TRDYN.
1-6	IRDYN (s/t/s)	I/O	Initiator RDY signal. It is shown that the data transmission preparation by the master side is ready. It becomes TS output in master mode, and becomes an input in target mode. It becomes possible only for FRAMEN assert term to output IRDYN.
1-7	STOPN (s/t/s)	I/O	Target end signal. A stop of a transaction is demanded from a master. It becomes an input in master mode, and becomes TS output in target mode.
1-8	DEVSELN (s/t/s)	I/O	Device selection signal. When the target device has recognized access, it asserts. IDSEL and FRAMEN assert at the time of a configuration, and when AD [1:0] is 00b (Type 0 config tran), it asserts. At the time of a usual transaction, the device is mapped to memory space at the time of FRAMEN assert, and an address hits, and when a command can be processed, it asserts. DEVSELN assert timing is Medium (after 2T from FRAMEN assert).

No.	Signal name	I/O	Function
1	**PCI Bus**		
1-9	IDSEL (in)	I	The device selection signal at the time of a configuration. At the time of FRAMEN assert, when IDESEL=H, AD[1:0] =00b and a command are config read or config write a device asserts DEVSELN and starts configration processing.
1-10	REQN (t/s)	O	PCI bus use request signal. REQN is asserted to arbitrator to use a bus by the master mode. It is set to TS at the time of RSTN assert.
1-11	GNTN (in)	I	PCI bus use permission signal. GNTN is asserted when arbitrator gives use permission by the master mode at the time of REQN assert. After it asserts GNTN and a master checks that a bus is IDLE (FRAMEN=H and IRDYN=H), it starts a transaction. The value of GNTN is disregarded at the time of RSTN assert.
1-12	CLK (in)	I	PCI clock signal. A maximum of 33MHz. When a device is performing internal processing which uses a PCI bus (an internal HOST_USEREQ flag is 1), CLK frequency of 33MHz is required. It is used by PCI interface block. Other internal blocks use SYSCLK signal which is another clock of 33MHz.
1-13	CLKRUNN (in,o/d)	I/O	Clock change / maintenance signal. While a device performs internal processing, the HOST_USEREQ flag is set to 1 by the case where the central resource set CLKRUNN to H and has notified change of the frequency of CLK a device asserts CLKRUNN 1T period, and requires a change failure of it.
1-14	RSTN (in)	I	PCI bus asynchronous reset signal. PCI interface block of a device is reset. A configration register returns to an initial state and REQN, AD, CBEN, and PAR become as TS. Moreover, GNTN in RSTN assert is disregarded. The internal MCORE block of those other than PCI interface is reset by a soft reset command or SYSRSTN signal, and is not reset by RSTN.
1-15	INTAN (o/d)	O	PCI Interrupt signal. When the interrupt phenomenon of a device occurs, about the phenomenon which has set the interrupt permission flag, INTAN is asserted and interruption processing is required of a system. INTAN signal is negateed when the interrupt flag of PCI IF block is cleared.

The direction and the state of PCI Bus signal are shown below.

In Target access, only when IDSEL, AD, and CBEN are checked and hit at the time of the assert of FRAMEN, DEVSELN is asserted and Target configuration transaction or Target memory transaction is started. Target can interpret and output a signal during the transaction. In Target access, the output of AD and TRDYN is possible at the time of the assert of DEVSELN, and PAR can be output to the term which delayed the assert of DEVSELN 1T, and while FRAMEN or IRDYN is asserting, the output is possible for STOPN. When Master has right to use a bus, it can interpret and output a signal.

	Pin name	I/O buf	Siganal polarity	RSTN	Un-cnfg	Target access		Master access	
						I/O	condition (related signal)	I/O	condition (related signal)
1	AD [31:0]	bi-dir (t/s)	--	in	in	I	Addr (FRAMEN asrt) Wdat (IRDYN & hit)	I	Rdat (TRDYN & DEVSELN)
						O	rdat (DEVSELN)	O	Addr (FRAMEN asrt) Wdat (IRDYN)
2	CBEN [3:0]	bi-dir (t/s)	H(com) L(ben)	in	in	I	Comm (FRAMEN asrt) Bena (IRDYN)	O	Comm (FRAMEN asrt) Bena (IRDYN)
3	PAR	bi-dir (t/s)	--	in	in	I	Addr (FRAMEN +1T) Wdat (DEVSELN+1T)	I	rddat (DEVSELN+1T)
						O	rddat (DEVSELN+1T)	O	Addr (FRAMEN +1T) Wdat (DEVSELN+1T)
4	FRAMEN	bi-dir (s/t/s)	L	in	in	I	hit transaction	O	bus idle (GNTN)
5	TRDYN	bi-dir (s/t/s)	L	in	in	O	data tran(DEVSELN)	I	data tran(DEVSELN)
6	IRDYN	bi-dir (s/t/s)	L	in	in	I	data tran(DEVSELN)	O	data tran(DEVSELN)
7	STOPN	bi-dir (s/t/s)	L	in	in	O	retry,disconnect (DEVSELN) abort (FRAMEN or IRDYN)	I	Target tran stop (FRAMEN or IRDYN)
8	DEVSELN	bi-dir (s/t/s)	L	in	in	O	hit transaction (FRAMEN or IRDYN)	I	target response (FRAMEN or IRDYN)
9	IDSEL	input (in)	H	in	in	I	Config access (FRAMEN assert)	NA	--
10	REQN	3-st out (t/s)	L	3-st	out	NA	--	O	bus request (when ms tran rdy)
11	GNTN	input (in)	L	in	in	NA	--	I	bus granted (REQN)
12	CLK	input (in)	(pos edge)	in	in	I	33MHz @host_usereq	I	same as target
13	CLKRUNN	bi-dir (in,o/d)	L	in	in	O	Rate change signal Keep 33MHz request (D0 & host_usereq)	O	same as target
14	RSTN	input (in)	L	in	in	I	PCI IF reset (anytime)	I	same as target
15	INTAN	3-st out (o/d)	L	3-st	3-st	O	IRQ singal (anytime)	O	same as target

No.	Signal name	I/O	Function
2	**Video Bus**		
2-1	VS	I	Vertical synchronized signal. At the time of ZV-port mode, it is used for discernment of a pause of a frame. In Digital Ycbus mode, it is for discernment of a pause of a field. Specification of the vertical effective range is set as a register via PCI. The assert polarity of VS is programmable. At the time of the ZV-port mode, one VS is asserted in one frame, and the assert timing (falling edge) shall be in the assert (H level) term of HS.
2-2	HS	I	Horizontal synchronized signal. It is used for discernment of a pause of the horizontal line. Specification of the horizontal effective range is set as a register via PCI. HS is used for the automatic refreshment timing of SDRAM. When HS pulses are not inputted more than 66 µsecs, It judges that HS is not inputted periodically and continues automatic refreshment of SDRAM using an internal counter. The assert polarity of HS is programmable.
2-3	PCLK	I	Video transmission clock. In ZV-port mode, this clock must be 14.318MHz and 12.27MHz in Digital YC bus mode. Each of YCDATs, HSs, and VS is PCLK synchronized signal.
2-4	YCDAT[15:0]	I/O	Pixel data. YUV(4:2:2) format. PCLK synchronized signal. In ZV-port progressive mode this bus is input. In Digital YC mode, input at the time of capture and output at the time of DOE active and display. Y data is transmitted to a higher byte, and UV data is transmitted to a low byte. The effective range of YCDAT is programmable. After SYSRSTN assert or soft reset, this bus becomes input mode.
2-5	ODD	I	The first field indication signal. It is used at the time of Digital YC interlace mode. It asserts during the ODD field. In not using ODD signal, fix to H externally.
2-6	DOE	O	YCDAT output indication signal. It is used at the time of Digital YC interlace mode. It asserts during the YCDAT output.
2-7	IICLK	O	External video CODEC initial cofiguration signal. It is used if needed.
2-8	IIDAT	I/O	External video CODEC initial cofiguration signal. It is used if needed. In TEST_MODE=L (normal operation) and SYSRSTN assert or soft reset command execution, it becomes output mode and in TEST_MODE=H (test mode) becomes I/O mode.

No.	Signal name	I/O	Function
3	**Mem Bus**		
3-1	MCKE	O	Memory clock enable signal. Connect to CKE pin of 16Mb SDRAM (524,288 x 16 x 2). Input same clock as SYSCLK to the CLK of SDRAM.
3-2	MCSN	O	Memory chip select signal. Connect to CSN pin of 16Mb SDRAM.
3-3	MRASN	O	Memory ROW address strobe signal. Connect to RASN pin of 16Mb SDRAM.
3-4	MCASN	O	Memory COLUMN address strobe signal. Connect to CASN pin of 16Mb SDRAM.
3-5	MWEN	O	Memory write enable signal. Connect to WEN pin of 16Mb SDRAM.
3-6	MADR[11:0]	O	Memory address signal. Connect to the A11-A0 pins of 16Mb SDRAM.
3-7	MDQ[15:0]	I/O	Memory data input/output siganl. Connect to the DQ15-DQ0 pin of the 16Mb SDRAM. It becomes output mode after SYSRSTN assert or soft reset command.
3-8	MDQM	O	Memory data input/output mask signal. Connect with LDQM and UDQM pins of 16Mb SDRAM. It is set to H level at the time after the assert of SYSRSTN signal, soft reset or soft reset of MCC, and it is set to L level after performing the power on sequence of SDRAM. This signal output L level except the above.

No.	Signal name	I/O	Function
4	**Miscellaneous**		
4-1	VB_MODE	I	Video Bus operation mode change signal. It becomes ZV_port progressive at the time of VB_MODE=L and Digital YC interlace at the time of H. Must be fixed before a power-on.
4-2	TEST_MODE	I	The test mode change signal of a chip. The signal used for LSI test at the time of shipment. It becomes normal operation mode at the time of TEST_MODE=L and becomes test mode at H. Must be fixed before power-on.
4-3	TAKE_PICN	I	The capture control signal in the camera mode. When asserting the MCORE_RDY flag, if this signal is asserted from the exterior, the one frame VGA picture will be captured to SDRAM. In this case, the initial cofiguration from a PCI bus is unnecessary. A TAKE_PICN input is disregarded during the MCORE_RDY negate. As for two or more captures in a MCORE_RDY assert term, only the last picture is saved. When a camera is OFF, TAKE_PICN is externally fixed to H.
4-4	MCORE_RDY	O	Indication signal of Capture operation. When capture operation is possible, H level is asserted, and it displays that a capture is possible. When one conditions of the followings are satisfied, it negates. 1) During the initialization term of SDRAM by hard reset or soft reset. 2) When there is no periodic input of HS signal (at the time of camera-off) 3) When LSI is set up in the low power mode

No.	Signal name	I/O	Function
4	**Miscellaneous**		
4-5	TCK	I	The terminal only for JTAGs. It is used for a test clock input. JTAG incoming signal is latched at the rising edge of TCK, and JTAG output signal changes at falling edge of TCK.
4-6	TMS	I	The terminal only for JTAGs. It is used for test mode selection. It is set to H level by the internal pull-up in the case of un-connecting.
4-7	TDI	I	The terminal only for JTAGs. It is used for a serial test data input. It is set to H level by the internal pull-up in the case of un-connecting.
4-8	TDO	O	The terminal only for JTAGs. It is used for a serial test data output. It is TS output signal.
4-9	TRST	I	The terminal only for JTAGs. It is used for test reset input. It is set to H level by the internal pull-up in the case of un-connecting.
4-10	SYSCLK	I	MCORE clock. 33MHz. Connect the same clock as the clock signal connected to MCLK pin of SDRAM. MCORE internal clock is disabled at the time of a low power mode.
4-11	SYSRSTN	I	MCORE reset signal. Hard reset of the circuits other than PCI interface block is carried out. From PCI side, the inside of MCORE can be initialized like the assert of SYSRSTN by performing a soft reset command. The initial cofiguration of SDRAM is performed after a reset end, and MCORE_RDY is asserted. RSTN of PCI is PCI interface block limitation, and reset of the other circuit is not performed.

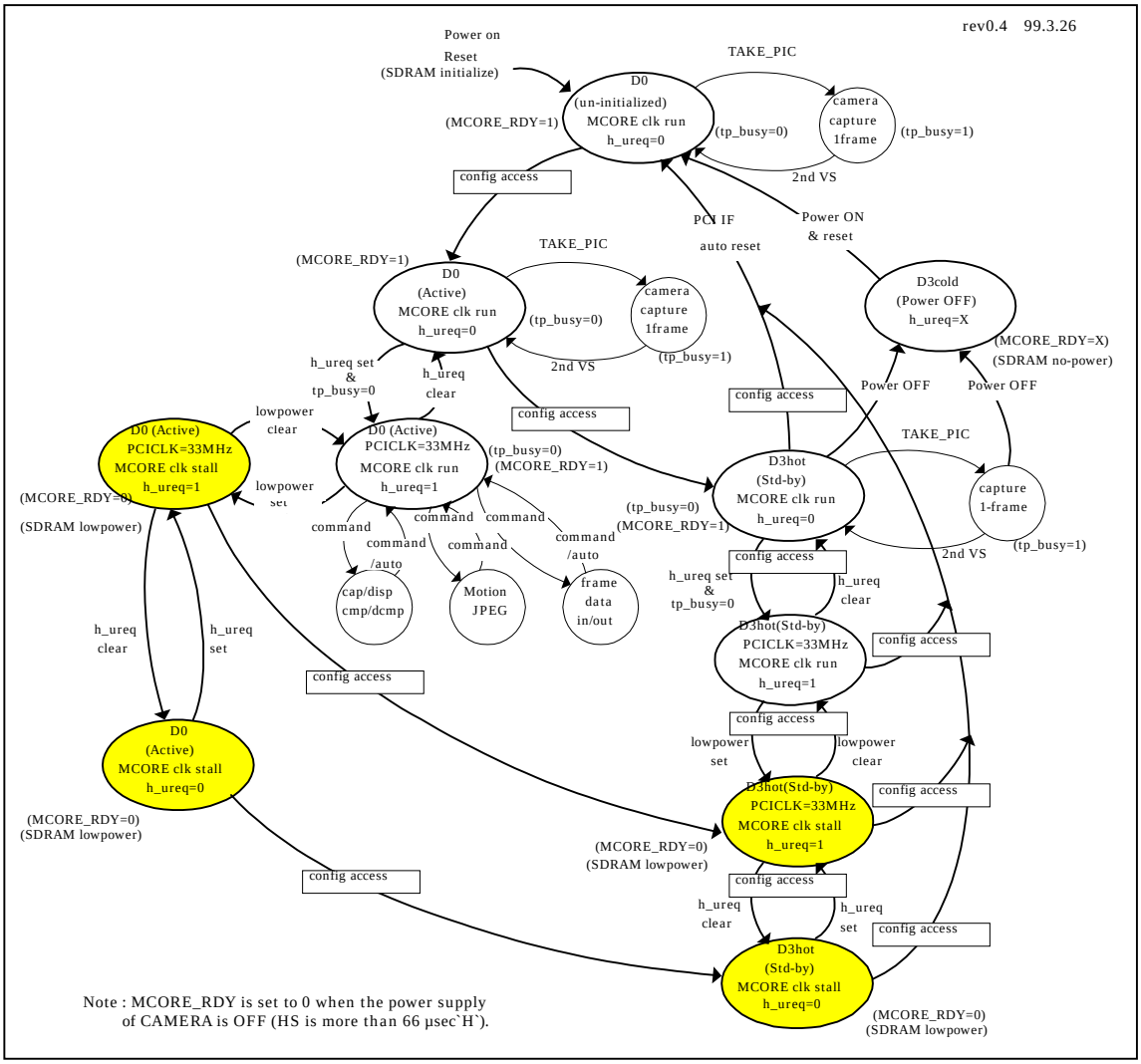
9. State transition diagram

Device status	PCI bus status	System status	HOST _USEREQ	Camera	Chip Process
D3cold (OFF)	B3 (OFF)	S5 (OFF) / S4 (Hybernation) / S3 (Suspend)	X	OFF	No Power
D0 (uninitial)	B0 (ON)	S0?	0	OFF MCORE_RDY=0	Power ON & PCIRST & SYSRST IDLE
				ON MCORE_RDY=1	Camera-Capture
D0 (Active)	B0 (ON) PCICLK=33MHz	S0 (WORKING)	0	OFF MCORE_RDY=0	IDLE
				ON MCORE_RDY=1	Camera-Capture
			1	OFF MCORE_RDY=0	IDLE
				ON Read still image MCORE_RDY=1	MJPEG Compression Pixel data continuous output
			1 LOWPOWER MCORE_RDY =0	OFF / ON	Low Power (stop MCORE clk)
	B1 (IDLE) CLK don't care	S1 (IDLE)	0	OFF MCORE_RDY=0	IDLE
				ON MCORE_RDY=1	Camera-Capture
			0 LOWPOWER MCORE_RDY =0	OFF / ON	Low Power (stop MCORE clk)
	B2 (NO CLK)		0	OFF MCORE_RDY=0	IDLE
				ON MCORE_RDY=1	Camera-Capture
			0 LOWPOWER MCORE_RDY =0	OFF / ON	Low Power (stop MCORE clk)
D3hot (Standby)	B0 (ON) CLK don't care	S0 (WORKING)	0	OFF MCORE_RDY=0	IDLE
				ON MCORE_RDY=1	Camera-Capture
	B1 (IDLE) CLK don't care	S1 (IDLE)		OFF MCORE_RDY=0	IDLE
				ON MCORE_RDY=1	Camera-Capture
	B2 (NO CLK)			OFF MCORE_RDY=0	IDLE
				ON MCORE_RDY=1	Camera-Capture

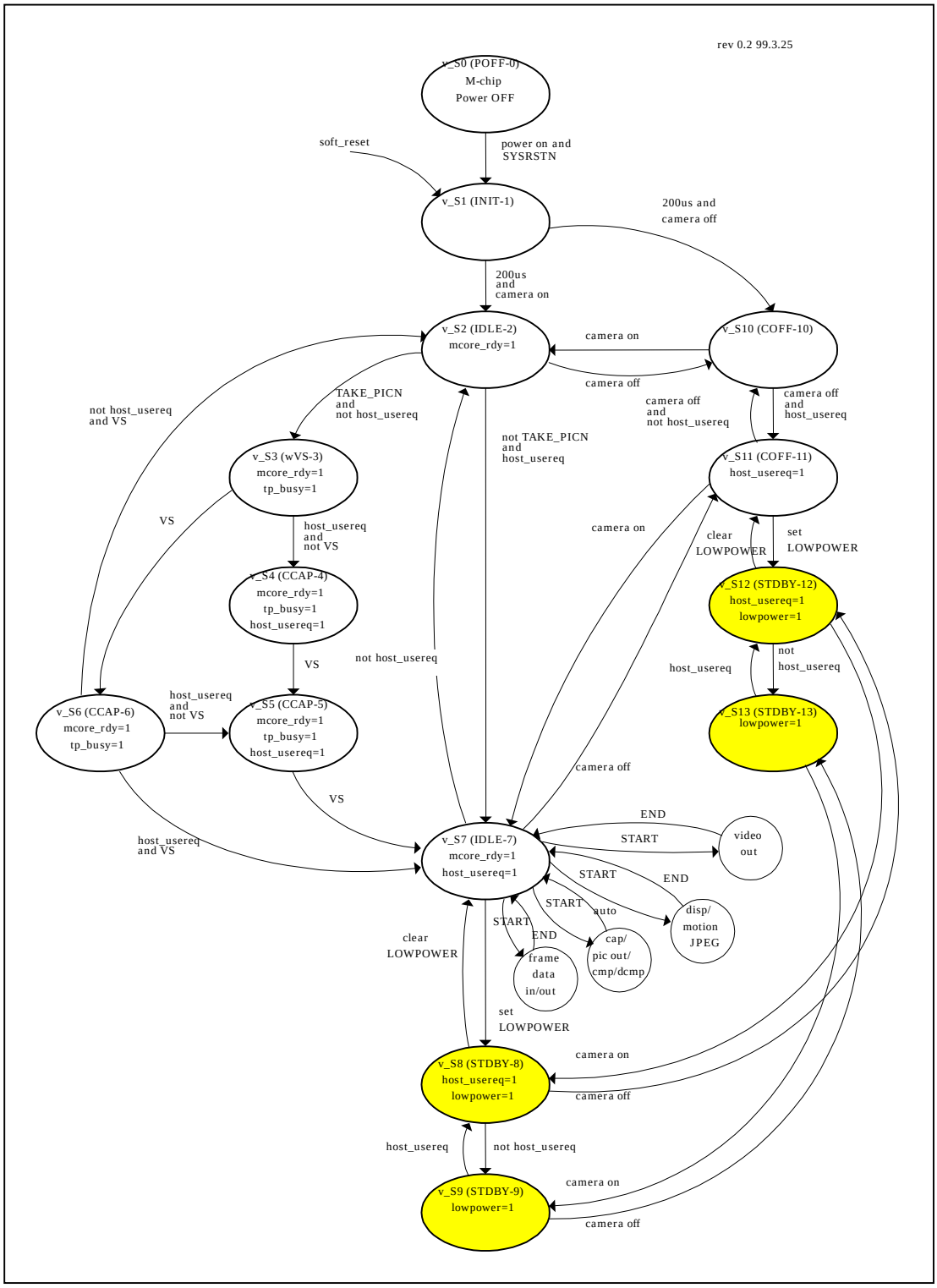
Note 1) MCORE_RDY is negateed at the time of the initial cofiguration after reset and reset. And also at the time of the low power mode and camera-off (HS pulse interval is 66 or more μsecs) .

2) When internal flag Host_usereq is 1, PCI CLK=33MHz is always demanded.

The device state D0-D3 transition diagram of a chip is shown below.



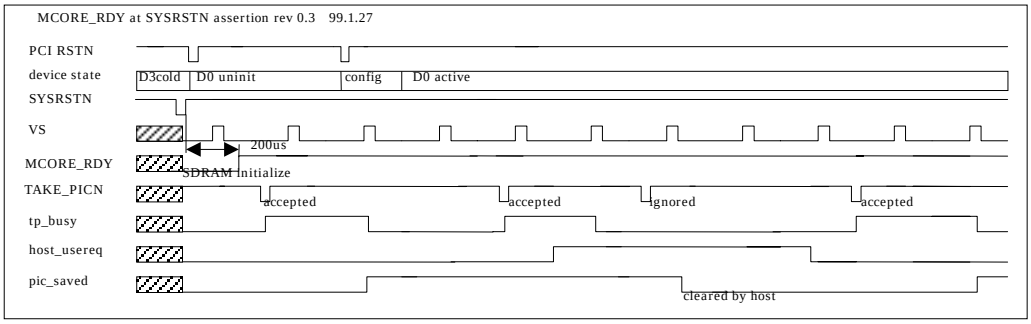
The device state transition diagram described about device processing state of a chip is shown below.



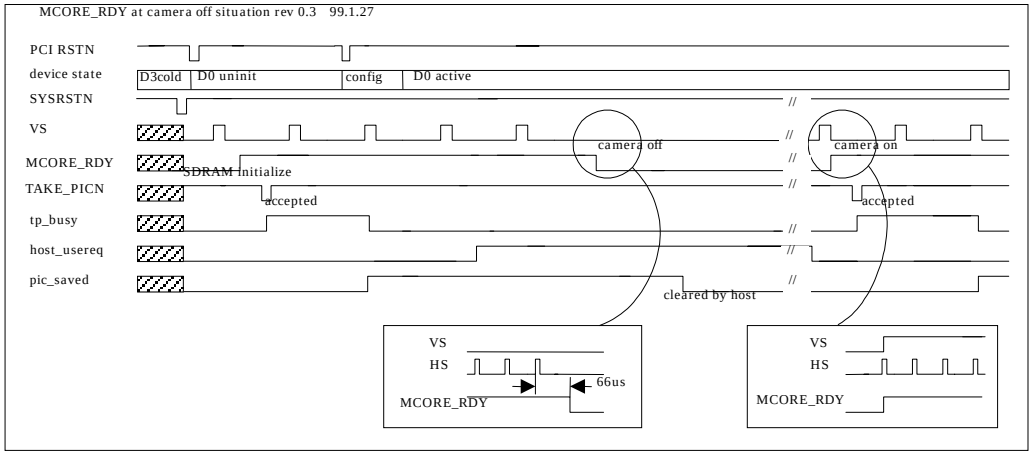
10. Timing diagram of outline of operation

Timing diagram of outline operation of MCORE_RDY signal is shown below.

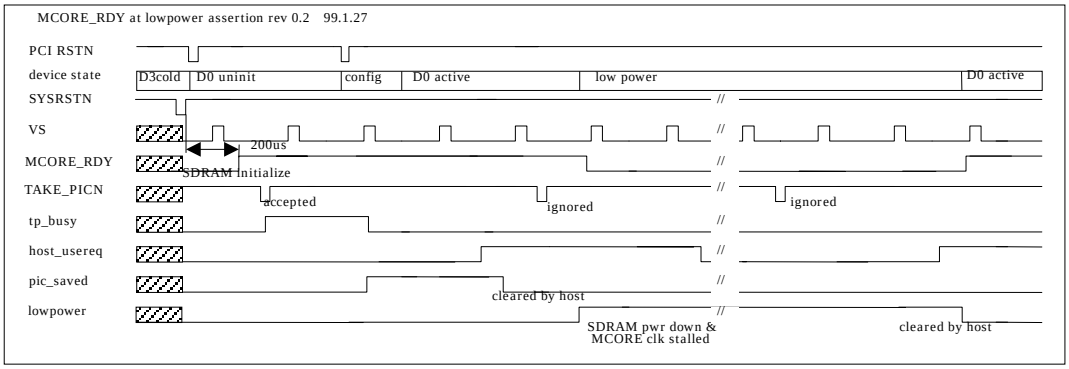
a) SYSRSTN assert timing



b) At the time of camera HS signal OFF

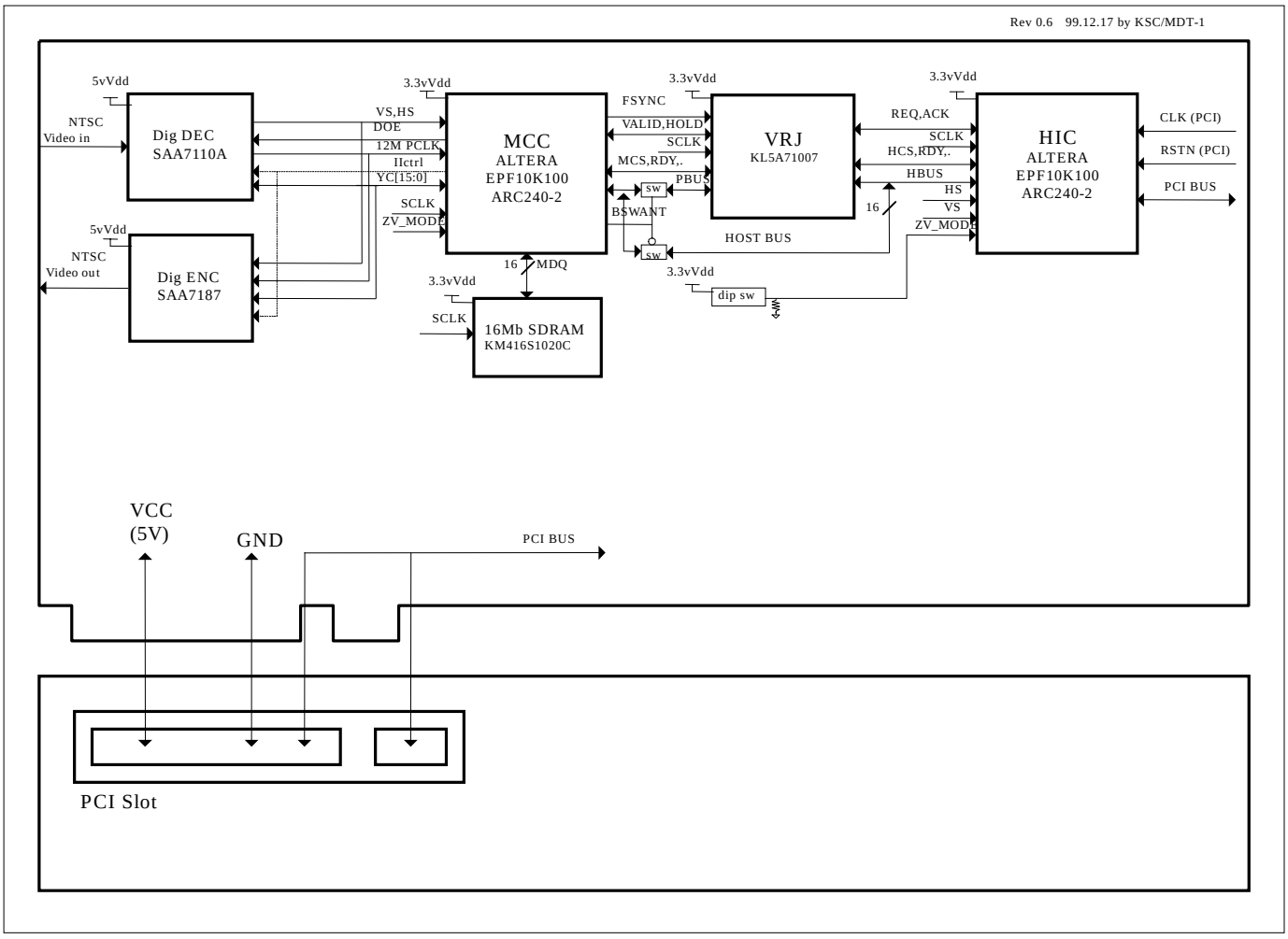


c) Low power mode



11. ALTERA evaluation board

Block diagram of Evaluation board of MJPEG is shown below.



12. Memory Map

The outline of MCORE register which mapped to the memory space of PCI and can be accessed in Target mode is shown below. Please refer to the 12.2, Memory Mapping Space (MCORE register) regarding the detail information about each registers.

a) PCI IF register

The control and the status register relevant to PCI transmission.

It is used at the time of the signal assert conditions of INTAN, and PCI Master operation.

Memory allocation information and a setup of the low power-consumption mode of MCORE.

b) HIC register

The control and the status register for using the data register for compression data transmission used at the time of PCI Target transmission, the status information on an internal block, and the automatic-control function of HIC.

c) MCC register

The register group about MCC among internal blocks.

When controlling LSI using the automatic-control function of HIC, access of this register group is unnecessary.

In accessing MCC register in PCI Target mode, read the status information on HIC register in advance, and can be accessed only when access is good.

d) VRJ register

The register group about JPEG core among internal blocks.

When controlling LSI using the automatic-control function of HIC, access of this register group is unnecessary.

In accessing VRJ register in PCI Target mode, read the status information on HIC register in advance, and access only when access is good.

The arrangement (memory map) on the memory space of each register group is shown below.

All the registers are alined to DoubleWord, and they are accessed per DW.

Although the base address has hit, about access to the address which is not effective, or the bit width which is not effective, it fillings in a bit 0 at the time of read-out, and is disregarded at the time of writing.

PCI Address (Offset)		Mapped register	Valid address range	Reset
[8:7]	[6]			
00b	0b	PCI IF register	000h – 020h	PCI RSTN D3 → D0 auto reset*
	1b	HIC register	040h – 07Ch	SYSRSTN or Soft-reset
01b	Xb	MCC register	080h - 0CCh	
1Xb	Xb	VRJ register	100h – 1F4h	

Note: In automatic reset of D3 →D0, SID, SVID, SIDC_EN, SID_COPY, and a SVID_COPY register are not cleared.

12.1 PCI configuration space

The outline and its initial value of PCI configuration header of LSI, mapped in the configuration space of PCI, which can be accessed in the Type 00h Configuration mode, and a device peculiar register are shown below.

Note : Access in the single data transmission mode to Configuration register.

As for access in the continuation data transmission mode, normal operation is not guaranteed.

No.	PCI Addr [7:0]	field	Bit width	R/W	Initial value	Comment
1	**00h**	**Vendor ID**	[15:0]	R	136Bh	Kawasaki Steel ID of PCI-SIG registration
2	**00h**	**Device ID**	[31:16]	R	FF01h	LSI device ID
3	**04h**	**Command**	[15:0]	R/W	0000h	
3-1		(reserved)	[15:10]	-	0000_00b	Read as 0, write ignored
3-2		(fast back2back)	[9]	R	0b	Not supported. Reserved.
3-3		(SERR# enable)	[8]	R/W	0b	1: Set the status[14] signed systemerror flag when address parity error occurs 0: signed system error unchanged Note: LSI is not supporting SERRN signal.
3-4		(Wait cycle ctrl)	[7]	R	0b	No stepping supported.
3-5		(Parity Err resp)	[6]	R/W	0b	1: error action enable - ms data p.e. flag set - target abort in case of address parity error 0: check disable (def) - ms data p.e. flag unchanged - tran continued in spite of address parity error Note:Although LSI is not supporting PERRN signal, it has parity generation and the detection function. Note: Correspondence at the time of parity error generating 1) set the detected parity error bit 2) at the time of address parity error -target abort if p.e.resp=1 -Processing is continued if resp=0. 3) at the time of data parity error - Processing is continued - set master data parity error flag if p.e.resp=1 - master data parity error flag unchanged if p.e.resp=0 Note: INTAN can be asserted by setup of the PCI IF IRQ status reg at the time of parity error.
3-6		(VGA Palet snoop)	[5]	R	0b	No palette registers.

No.	PCI Addr [7:0]	field	Bit wirth	R/W	Initial value	comment
3-7		(Mem write & invld) (MWI_enable)	[4]	R/W	0b	mem wr & invalidate support bit 1: MWI command used when write 0: mem write used (def) Note: even if MWI=1, Cache Line Size reg is not 8DW, mem write will be used when master write.
3-8		(Special cyc resp)	[3]	R	0b	No action on `special cycle`
3-9		(Master Mode Ena)	[2]	R/W	0b	Master action enable bit. 1: master action enable 0: master action disable (def)
3-10		(Mem space mapped)	[1]	R/W	0b	Memory space mapped flag. 1: device mapped to Mem space 0: device unmapped (def)
3-11		(IO space mapped)	[0]	R	0b	I/O space mapping not supported.
4	**04h**	**Status**	[31:16]			Can be read normally Only the bit which wrote 1 is cleared by 0 in Write. As for the bit which writes in 0, the value will not change.
4-1		(Detected Par Err)	[31]	R/W	0b	Parity Error detect flag 1: PE detected (despite of 3-5) - target addr parity error - target data p.e. @wr tran - master data p.e. @rd tran 0: no PE detect (def)
4-2		(Signaled Sys Err)	[30]	R/W	0b	Signed System error flag 1: address PE detected When Command [8, 6] is set and Address PE occurs 0: no SERR detect (def)
4-3		(MasterAbort rcvd)	[29]	R/W	0b	Master Abort occurred (MS only) 1: MS abort termination occurred 0: no MS abort (def)
4-4		(TargetAbort rcvd)	[28]	R/W	0b	Target Abort occurred (MS only) 1:TGTabort termination occurred 0: no TGT abort (def)
4-5		(Signaled TGTabrt)	[27]	R/W	0b	Target Abort occurred (TGT only) 1:TGTabort termination occurred 0: no TGT abort (def)
4-6		(DEVSELN timing)	[26:25]	R	01b	DEVSEL assert timing is medium except for configuration

No.	PCI Addr [7:0]	field	Bit wirth	R/W	Initial value	comment
4-7	04h	(master data parity error)	[24]	R/W	0b	Master only set if Parity Err resp. is set and p.e. detected. 1: PE detected during MS read 0: no PE occurred (def) Note: PERRN is NOT supported
4-8		(fast bck2bck cap)	[23]	R	0b	Not b2b capable as TGT device
4-9		(UDF supported)	[22]	R	0b	No specific user defined config
4-10		(66MHz capable)	[21]	R	0b	Device is 33MHz operation
4-11		**(PMI capability)**	[20]	R	1b	Power Management capability supported
4-12		reserved	[19:16]	R	0000b	Reserved
5	**08h**	**Revision ID**	[7:0]	R	01h	LSI revision ID
6	**08h**	**Class Code**	[31:8]	R	04_8000h	
6-1		(general class)	[31:24]	R	04h	Multimedia device
6-2		(sub-class)	[23:16]	R	80h	Not audio nor video MM device
6-3		(RL program if)	[15:8]	R	00h	
7	**0Ch**	**Cache Line Size (CLS)**	[7:0]	R/W	00h	Set burst trans. data volume('DW) In master write, if CLS=8 & MWI_enable=1 ms write & invalidate used else master write command used; In master read, if CLS=8 & MRL_en(PCI_IF)=1 master read line com used else master read command used;
8	**0Ch**	**Latency Timer**	[15:8]	R/W	00h	
8-1		(prog'd Latency)	[15:11]	R/W	0_0000b	N by 8T time limit programmable.
8-2		(granuality 8T)	[10:8]	R	000b	Fixed value.
9	**0Ch**	**Header Type**	[23:16]	R	00h	
9-1		(multi function)	[23]	R	0b	Single function only
9-2		(header type)	[22:16]	R	000_0000b	Type 00h header supported
10	**0Ch**	**BIST**	[31:24]	R	00h	Built-In-Self-Test not supported
11	**10h**	**Base Address Reg**	[31:0]	R/W	0000_0000h	Base address for memory space
11-1		(mem size request)	[8:4]	R	0_0000b	Required 512Bytes memory space
11-2		(prefetchable)	[3]	R	0b	Data is not prefetchable
11-3		(prefetchable)	[3]	R	0b	Data is not prefetchable
11-4		(Base reg type)	[2:1]	R	00b	32bit wide and locate anywhere.
11-5		(Mem sp indicate)	[0]	R	0b	Base reg for memory
12	14h	reserved	[31:0]	R	0000_0000h	Not used this area
13	18h	reserved	[31:0]	R	0000_0000h	Not used this area
14	1Ch	reserved	[31:0]	R	0000_0000h	Not used this area
15	20h	reserved	[31:0]	R	0000_0000h	Not used this area
16	24h	reserved	[31:0]	R	0000_0000h	Not used this area
17	28h	Cardbus CIS pointr	[31:0]	R	0000_0000h	Not support CardBus usage
18	**2Ch**	**Subsystem VendorID (SVID)**	[15:0]	R/W *	136Bh (same as Vendor ID)	* conditional writable register if write to SVID_COPY SVID_COPY= wr_data SVID = wr_data; if write to SVID if SIDC_EN=1 SVID_COPY= wr_data SVID = wr_data else SVID, SVID_COPY unchanged; Note: SVID,SVID_COPY, SIDC_EN is not cleared at D3→D0

No.	PCI Addr [7:0]	field	Bit wirth	R/W	Initial value	comment
19	**2Ch**	**Subsystem ID (SID)**	[31:16]	R/W *	FF01h (same as Device ID)	* conditional writable register if write to SID_COPY SID_COPY= wr_data SID = wr_data; if write to SID if SIDC_EN=1 SID_COPY= wr_data SID = wr_data else SID, SID_COPY unchanged; Note: SID,SID_COPY, SIDC_EN Is not cleared at D3→D0
20	**30h**	**Expansion ROM BA**	[31:0]	R	0000_0000 h	Not supported
21	**34h**	**PM capability ptr (CAP_PTR)**	[7:0]	R	50h	Power Management capability Linked list location pointer
22		reserved	[31:8]	R	00_0000h	reserved
23	38h	reserved	[31:0]	R	0000_0000 h	reserved
24	**3Ch**	**Interrupt Line**	[7:0]	R/W	00h	Interrupt routing info reg. INTAN supported.
25	**3Ch**	**Interrupt Pin**	[15:8]	R	01h	INTAN supported
26	**3Ch**	**Min_Gnt**	[23:16]	R	3h	How long of burst period (0.25usec unit) 8DW with no wait needs around 0.3usec.
27	**3Ch**	**Max_Lat**	[31:24]	R	6h	How often device like granted (from REQ assert to next REQ) (0.25usec unit) LSI assert REQ as soon as 8DW FIFO is ready to transfer.

The configuration register of a device peculiar domain is shown below.

No.	PCI Addr [7:0]	field	Bit wirth	R/W	Initial value	comment
U1	**40h**	**SID,SVID write Enable (SIDC_EN)**	[0]	R/W	0b	SID or SVID reg write enable 1: SID or SVID writable 0: SID or SVID read only (def) Note: SID,SVID,SIDC_EN is not cleared at D3→D0
U2		reserved	[31:1]	R	0000_0000 h	reserved
U3	**44h**	**SVID copy reg (SVID_COPY)**	[15:0]	R/W	0000h	SVID copy register. Write data also load to SVID. Note: SVID_COPY,SVID,SIDC_EN is not cleared at D3→D0
U4	**44h**	**SID copy reg (SID_COPY)**	[31:16]	R/W	0000h	SID copy register. Write data also load to SID. Note: SID_COPY,SID,SIDC_EN is not cleared at D3→D0
U5	**48h**	**Sub revision ID**	[7:0]	R	01h	Chip minor revision
U6		reserved	[31:8]	R	00_0000h	reserved
U7	4Ch	reserved	[31:0]	R	0000_0000 h	reserved
U8	**50h**	**Capability ID**	[7:0]	R	01h	PM reg linked list top
U9	**50h**	**Next Item Pointer**	[15:8]	R	00h	No additional items
U10	**50h**	**PM capabilities**	[31:16]	R	0000_0002 h	
U10-1		(PME support)	[31:27]	R	0_0000b	No PME# supported
U10-2		(D2 support)	[26]	R	0b	D2 state not supported
U10-3		(D1 support)	[25]	R	0b	D1 state not supported
U10-4		(Aux current req)	[24:22]	R	000b	No PME# supported
U10-5		(DevSpecific Init)	[21]	R	0b	Windows driver not use this bit
U10-6		reserved	[20]	R	0b	reserved
U10-7		(PME clock)	[19]	R	0b	No PME# supported
U10-8		(PMI spec version)	[18:16]	R	010b	PCI PM Interface Spec rev 1.1
U11	**54h**	**PM control/status**	[15:0]	R/W	0000h	
U11-1		(PME status)	[15]	R	0b	No PME# supported
U11-2		(Data scale)	[14:13]	R	00b	No data register (UC) supported
U11-3		(Data select)	[12:9]	R	0000b	No data register (UC) supported
U11-4		(PME enable)	[8]	R	0b	No PME# supported
U11-5		(reserved)	[7:2]	R	00_0000b	reserved
U11-6		(Power state)	[1:0]	R/W	00b	Device power state & control 00b: D0 (def) 11b: D3hot otherwise: change ignored Note: if 01b or 10b value is write this register, tran is completed and value unchanged. Note: if power_state changes from 11b to 00b, all PCI IF reg including configuration reg, excluding 2Ch,40h,44h will be reset internally.
U12	**54h**	**PMCSR bridge support extensions**	[23:16]	R	00h	Device not PCI2PCI bridge
U13	**54h**	**Data register**	[31:24]	R	0000h	Not supported
U14	58h	reserved	[31:0]	R	0000_0000 h	reserved
U15	5Ch	reserved	[31:0]	R	0000_0000 h	reserved

The following is a configuration register used for LOWPOWER setup and release by PCI configuration access. The handling of each flag is based on the processing by HIC register.

No.	PCI Addr [7:0]	field	Bit wirth	R/W	Initial value	comment
U16	**60h**	**MCORE_STATUS**	[5:0]	R	-	Alias of HIC status flag bits.
U16-1		HOSTUSEREQ_STATUS	[0]	R	-	Alias of HIC HOST_USEREQ bit.
U16-2		TPBUSY_STATUS	[1]	R	-	Alias of HIC TP_BUSY bit.
U16-3		PICSAVED_STATUS	[2]	R	-	Alias of HIC PIC_SAVED bit.
U16-4		LOWPOWER_STATUS	[3]	R	-	Alias of HIC LOWPOWER bit.
U16-5		HICST4_STATUS	[4]	R	-	Alias of HIC STATUS[4] bit.
U16-6		MCORERDY_STATUS	[5]	R	-	Alias of HIC MCORERDY_FLAG bit.
U17		reserved	[31:6]	R	000_0000h	reserved
U18	**64h**	**HOSTUSEREQ_SET**	[0]	R/W	0b	Auto clear. Writing 0 no-effect. Writing 1 set HIC HOST_USEREQ.
U19		reserved	[31:1]	R	0000_0000h	reserved
U20	**68h**	**HOSTUSEREQ_CLR**	[0]	R/W	0b	Auto clear. Writing 0 no-effect. Writing 1 clear HIC HOST_USEREQ.
U21		reserved	[31:1]	R	0000_0000h	reserved
U22	**6Ch**	**LOWPOWER_SET**	[0]	R/W	0b	Auto clear. Writing 0 no-effect. Writing 1 set HIC LOWPOWER.
U23		reserved	[31:1]	R	0000_0000h	reserved
U24	**70h**	**LOWPOWER_CLR**	[0]	R/W	0b	Auto clear. Writing 0 no-effect. Writing 1 clear HIC LOWPOWER.
U25		reserved	[31:1]	R	0000_0000h	reserved
U26	**74h**	**SOFTRESET_SET**	[0]	R/W	0b	Auto clear. Writing 0 no-effect. Writing 1 set HIC SOFT_RESET bit.
U27		reserved	[31:1]	R	0000_0000h	reserved
U28	**78h**	**SCRATCH_PAD**	[7:0]	R/W	00h	Just in case.
U29		reserved	[31:8]	R	00_0000h	reserved

12.2 Memory Mapping space (MCORE register)

No.	Register name	Addr [8:0]	R/W	Bit field		Function
1	PCI IF register					
1-1	PCI mode	00h [00dw]	R/W	PCI_MODE[2:0]		Set the operation mode of PCI PCI_MODE[0] must be set 1:Retry mode (def)
				[0]	1:Retry mode (def) 0: reserved	
				[1]	0: Master mode (def) 1: Not master mode	
				[2]	0: mem read @ master read 1: mem read line @ master read (def)	External memory read-out command selection at a master mode Use the memory read line command at CLS reg=8 of config space
1-2	IRQ status	04h [01dw]	R	INTA[14:0]		All the flag of bit [6:0] is cleared by read-out
				[0]	MCC IRQ flag (def 0)	It is set to 1 at the IRQ assert time of MCC.
				[1]	VRJ IRQ flag (def 0)	It is set to 1 at the IRQ assert time of VRJ.
				[2]	1 frame HIC processing end flag (def 0)	It is set to 1 when the compression and de-compression processing for one frame are completed.
				[3]	HIC_END flag (def 0)	It is set to 1 when processing of HIC is completed.
				[4]	Error flag (def 0)	It is set to 1 when JPEG de-compress error occurs.
				[5]	Capture end (def 0)	It is set to 1 when capture processing is completed
				[6]	PCI error/abort flag	Monitoring the followings during the PCI transaction. 1) parity error (not supported) 2) system error (not supported) 3) ms abort (master mode) 4) target abort (master mode) 5) target abort (target mode) This flag is set to 1 when either of the status reg 04h [31:27] of config asserts 1. It can judge by which item it set by reading status reg of config.
				[7]	reserved	Read as 0
			R/W	[8]	reserved (def 0)	When the flag enable bit of bit [14:8] is 0, the corresponding flag is not concerned with the existence of an event, but is always set to 0.
				[9]	reserved (def 0)	
				[10]	1:Bit2 enable 0:Bit2 read as 0 (def)	
				[11]	1:Bit3 enable 0:Bit3 read as 0 (def)	
				[12]	1:Bit4 enable 0:Bit4 read as 0 (def)	
				[13]	reserved (def 0)	
				[14]	1:Bit6 enable 0:Bit6 read as 0 (def)	
1-3	Page Table Address pointer	08h [02dw]	R/W	PT_ADDR[31:12]		The base address which stored the page list which can be used at the time of PCI master transmission.

No.	Register name	Addr [8:0]	R/W	Bit field		Functions
1	PCI IF register					
1-4A	Frame information 1 FIR1 (continuous compression and de-compression)	0Ch [03dw]	R/W	F_INFO1[31:0]		Use at PCI master transfer.
				[0]	0: Possible to write frame. (def) 1: Possible to read frame.	Frame output (compression) 0:possible to access frame area (output) 1: End of frame data output / release waiting At master mode input (de-comp.) 0: waiting for frame data preparation / end of access 1: Frame domain use (input) is possible.
				[10:1]	The amount of DWs of an end page (def 0)	Used only at frame output (compression).
				[18:11]	End PAGE_TABLE ID (def 0)	Used at the master input and an output.
				[26:19]	Start PAGE_TABLE ID (def 0)	
				[31:27]	Number of lost Frames (def 0)	Used only at the frame output (compression).
1-4B	Frame information 1 FIR1 (continuous pixel output)	0Ch [03dw]	R/W	F_INFO1[31:0]		
				[0]	0: Possible to use frame domain (def). 1:End of frame data output	
				[16:1]	N/A. Value is not defined. (def 0)	
				[26:17]	Start PAGE_TABLE ID (def 0)	
				[31:27]	Number of lost frames. (def 0)	
1-5A	Frame information 2 FIR2 (continuous compression and de-comp.)	10h [04dw]	R/W	F_INFO2[31:0]		Refer to 1-4A
				[0]	0: Possible to write frame. (def) 1: Possible to read frame.	
				[10:1]	Data volume of end page. (def 0)	
				[18:11]	End PAGE_TABLE ID (def 0)	
				[26:19]	Start PAGE_TABLE ID (def 0)	
				[31:27]	Number of lost frames. (def 0)	
1-5B	Frame information 2 FIR2 (continuous pixel output)	10h [04dw]	R/W	F_INFO2[31:0]		
				[0]	0: Possible to use frame domain (def). 1:End of frame data output	
				[16:1]	N/A. Value is not defined. (def 0)	
				[26:17]	Start PAGE_TABLE ID (def 0)	
				[31:27]	Number of lost frames. (def 0)	
1-6A	Frame information 3 FIR3 (continuous compression and de-comp.)	14h [05dw]	R/W	F_INFO3[31:0]		Refer to 1-4A
				[0]	0: Possible to write frame. (def) 1: Possible to read frame.	
				[10:1]	Data volume of end page. (def 0)	
				[18:11]	End PAGE_TABLE ID (def 0)	
				[26:19]	Start PAGE_TABLE ID (def 0)	
				[31:27]	Number of lost frames. (def 0)	
1-6B	Frame information 3 FIR3 (continuous pixel output)	14h [05dw]	R/W	F_INFO3[31:0]		
				[0]	0: Possible to use frame domain (def). 1:End of frame data output	
				[16:1]	N/A. Value is not defined. (def 0)	
				[26:17]	Start PAGE_TABLE ID (def 0)	
				[31:27]	Number of lost frames. (def 0)	

No.	Register name	Addr [8:0]	R/W	Bit field		Functions
1	PCI IF register					
1-7A	Frame information 4 FIR4 (continuous compression and de-comp.)	18h [06dw]	R/W	F_INFO4[31:0]		Refer to 1-4A
				[0]	0: Possible to write frame. (def) 1: Possible to read frame.	
				[10:1]	Data volume of end page. (def 0)	
				[18:11]	End PAGE_TABLE ID (def 0)	
				[26:19]	Start PAGE_TABLE ID (def 0)	
				[31:27]	Number of lost frames. (def 0)	
1-7B	Frame information4 FIR4 (continuous pixel output)	18h [06dw]	R/W	F_INFO4[31:0]		
				[0]	0: Possible to use frame domain (def). 1:End of frame data output	
				[16:1]	N/A. Value is not defined. (def 0)	
				[26:17]	Start PAGE_TABLE ID (def 0)	
				[31:27]	Number of lost frames. (def 0)	
1-8	PCI TGT data	1Ch [07dw]	R/W	FIFO_REG[31:0]		The register for data access at the PCI Target transmission mode. Not used at Master transmission mode. Check PCI TGT data status before access. Only this register is reset by MCORE soft reset processing among PCI IF registers.
1-9	PCI TGT data status	20h [08dw]	R	FIFO_STATUS[1:0]		Before accessing PCI TGT data register, PCI TGT data status is surely checked each time, and data transmission is performed only when value is 3.
				[1:0]	0: HIC idle (tran done) (def) 1: HIC idle (tran done) 2: FIFO wait request 3: FIFO data ready	

Note 1) F_INFO[0] -- At the time of an output, the external memory storing information on outputted frame data is displayed. If the memory storing information on frame data which should be read from the exterior is specified, the corresponding memory position will be accessed one by one, and it will input into a chip.

2) F_INFO[31:27] -- The number of lost frames from the last frame output to this time is recorded.

3)access to the F_INFO at continuous processing –

The value of 0 bit each of F_INFO1 to 4 is checked, and the page which can be used is accessed one by one.

F_INFO is a ring buffer, so wait till it becomes possible to access when next F_INFO can not be access.

No.	Register name	Addr [8:0]	R/W	Bit field		Functions
2	HIC register (possible to Read/Write at LOWPOWER mode)					
2-1	HOST_USEREQ	40h [10dw]	R/W	HOST_USEREQ[0]		Camera capture permission flag. When HOST_USEREQ is H, a TAKE_PIC signal becomes invalid. Besides the set-reset by memory access, a HOST_USEREQ bit can be set, clear and monitor by PCI configuration access. A HOST_USEREQ bit will be set if 1 is written to 64h [0] of config space by Config write. Moreover, a HOST_USEREQ bit will be cleared if 1 is written to 68h [0]. The state of a HOST_USEREQ bit can be checked by reading 60h [0] of config space. Neither the assert of PCI RSTN nor the automatic PCI IF reset at D3 → D0 affects the state of a HOST_USEREQ bit.
				[0]	0:TAKE_PIC valid (def) 1:PCI host request to use MCORE	
2-2	TP_BUSY	44h [11dw]	R	TP_BUSY[0]		This bit is set to 1 at the time of a TAKE_PIC assert, and cleared by 0 after MCORE ends camera capture processing. This bit can be monitored by reading 60h[1] at config read.
				[0]	0:IDLE (def) 1: Under camera capture execution	
2-3	PIC_SAVED	48h [12dw]	R/W	PIC_SAVED[0]		This bit is set to 1 only when a picture is taken in to SDRAM by TAKE_PIC (camera capture), and cleared if 0 is written in from the exterior. Can be monitored by reading 60h [2] by Config read.
				[0]	0: no camera captured picture in SDRAM (def) 1: camera captured picture in SDRAM	
2-4	LOWPOWER	4Ch [13dw]	R/W	LOWPOWER[0]		If LOWPOWER bit is set to 1, SDRAM will be set as the power down mode, SYSCLK is fixed to H level inside, and it becomes the low power-consumption mode. If a bit is cleared to 0, the mask of SYSCLK will be canceled and normal operation will be possible. Cleared by SYSRSTN assert. The data of SDRAM are not held during the power down. Besides the set and reset by memory access, LOWPOWER bit is set, cleared and monitored by PCI configuration access LOWPOWER bit will be set if 1 is written to 6Ch[0] of config space by Config write. Moreover, LOWPOWER bit will be cleared if 1 is written to 70h [0]. The state of LOWPOWER bit can be checked by reading 60h [3] of config space. Neither the assert of PCI RSTN nor the automatic PCI IF reset at D3 → D0 affects the state of LOWPOWER bit.
				[0]	0: Normal mode (def) 1: Stop internal clock of MCORE	

No.	Register name	Addr [8:0]	R/W	Bit field		Functions
2	HICregister (possible Read/Write even at LOWPOWER mode)					
2-5	SOFT_RESET	50h [14dw]	R/W	SOFT_RESET[0]		If a SOFT_RESET bit is set to 1, 2T term reset will be performed to the inside of MCORE, and HIC register, MCC register, and VRJ register will be initialized. A SOFT_RESET bit is automatically cleared to 0 after ending reset of an internal register, and external SDRAM is initialized. If SOFT_RESET is performed, MCORE will be in an initial state also in the time of LOWPOWER. A SOFT_RESET bit will be set if 1 is written to 74h [0] of config space by Config write.
				[0]	0: normal mode (def /auto-clear) 1: reset to MCORE	
	MCORERDY_FLAG		R	MCORERDY_FLAG[1]		Alias flag of MCORE_RDY MCORE_RDY is set to L at the following conditions. 1. SYSRST assert 2. soft reset 3. 200us term after reset 4. initial cofiguration of SDRAM 5. camera-off (when negateing 66 usec or more of HS pulses) 6. LOWPOWER assert
				[1]	0: MCORE_RDY= L 1: MCORE_RDY= H (def)	

No.	Register name	Addr [8:0]	R/W	Bit field		Functions
2	HIC register (possible to read even at LOWPOWER mode)					
2-6	HIC command	54h [15dw]	R/W	HIC_COMMAND[1:0]		
				[1:0]	0h:NO-OP(def/auto-clear) 1h:HIC_MODE processing start bit The processing set as HIC_MODE is started. 2h: HIC_MODE processing end bit The following continuation commands are ended among the commands set as HIC_MODE. HIC_MODE= 2h,5h,6h,8h Otherwise: Invalid command (NO-OP)	Don't write to this register at LOWPOWER mode
2-7	HIC mode	58h [16dw]	R/W	HIC_MODE[3:0]		
				[3:0]	0h: Invalid command (NO-OP) (def) 1h: still image capture 2h: display 3h: still image compression 4h: still image de-compression 5h: continuous capture & compression 6h: continuous de-compression & display 7h: still image output 8h: continuous image output otherwise: Invalid command (NO-OP)	Don't write to this register at LOWPOWER mode
2-8	status	5Ch [17dw]	R	HIC_STATUS[4:0]		HIC_STATUS[1:0] is used for direct access to each sub-modules. [4] is set to 1 when HIC is executing the command (camera capture execution, TP_BUSY=1 is included). At this time, when commands are a capture/display, it asserts [2] and HIC is performing compression / de-compression processing, asserts [3]. At the time of HIC idle and a processing normal end, HIC_STATUS[4:0] is set to 03h. If HIC starts processing in mode setup 3 to 8h, HIC_STATUS [1:0] will be 00b until it ends processing and it will become impossible to access MCC and VRJ register.
				[0]	1: Possible to access to MCC register (def) 0: Impossible to access to MCC register	
				[1]	1: Possible to access to VRJ register (def) 0: Impossible to access to VRJ register	
				[2]	1: Under a capture / display command execution 0: Picture input-and-output processing end (def)	
				[3]	1: Under compression / de-compression processing command execution 0: Compression / de-compression processing end (def)	
				[4]	1: Under HIC command execution 0:HIC idle (def)	
2-9	Process-ing rate	60h [18dw]	R/W	S_RATE[4:0]		The frames processing rate of Motion-JPEG operation is specified. It processes by skipping a number of specified frames.
				[4:0]	0h:every frame procesing (def) Nh: every N frame procesing (N can be set 0 to 31)	
2-10	Picture output form	64h [19dw]	R/W	PCI_VIDEOFMT[0]		The picture data output form to the PCI bus at the time of a still picture output and a continuation picture output is specified.
				[0]	0h:{B3,B2,B1,B0}={V,Y',U,Y} (def) 1h: {B3,B2,B1,B0}={Y',V,Y,U}	

No.	Register name	Addr [8:0]	R/W	Bit field	Functions
2	HIC register – use only for test (Never access during the normal operation)				
2-11	TEST REG 1	68h [1Adw]	R	HIC_TESTSTATUS1[31:0]	Status register for test
2-12	TEST REG 2	6Ch [1Bdw]	R	HIC_TESTSTATUS2[31:0]	Status register for test
2-13	TEST REG 3	70h [1Cdw]	R	HIC_TESTSTATUS3[31:0]	Status register for test
2-14	TEST REG 4	74h [1Ddw]	R	HIC_TESTSTATUS4[31:0]	Status register for test
2-15	TEST REG 5	78h [1Edw]	R	HIC_TESTSTATUS5[31:0]	Status register for test
2-16	TEST REG 6	7Ch [1Fdw]	R/W	HIC_TESTCONTROL[31:0]	Status register for test Never access during the normal operation

No.	Register name	Addr [8:0]	R/W	Bit field		Functions
3	MCC register					
3-1	MCC command	80h [20dw]	R/W	MCC_COM[3:0]		It is used when accessing MCC directly. Usually, HIC performs an automatic setup and controls MCC. MCC soft reset command performs same processing as SYSRSTN of LSI and the soft reset to MCC block. MDQM is asserted to H to SDRAM 200uses period, and it initializes after that.
				[3:0]	0h: Initial value setup (def) 1h: IIC setting start 2h: IIC setting end 3h: FM writing 4h: FM read-out 5h: FM access stop 6h: Capture 7h: display 8h: Display end 9h: still image compression Ah: still image de-compression Bh: still image output Ch: continuous image output Dh: continuous compression Eh: continuous de-compression Fh: MCC softreset	
3-2	IIC_WRITE	84h [21dw]	W	IIC_WRREG[7:0]		Used at initial cofiguration of external Video Codec.
3-3	MCC_WRITE	88h [22dw]	W	MCC_WRREG[15:0]		Used at the data writing to MCC.
3-4	MCC_READ	8Ch [23dw]	R	MCC_RDREG[15:0]		Used at the data read-out from MCC.
3-5	MCC status	90h [24dw]	R	MCC_STATUSREG[7:0]		
				[0]	1: Under capture processing 0: Capture processing end (def)	
				[1]	1: Under display processing 0: Display processing end (def)	
				[2]	1: Under compression processing (image data output) 0: Compression processing end (def)	
				[3]	1: Under de-compression processing (image data input) 0: De-compression processing end (def)	
				[4]	1:MCC_WRREG access is possible. 0: MCC_WRREG access is impossible. (def)	
				[5]	1: MCC_RDREG access is possible. 0: MCC_RDREG access is impossible. (def)	
				[6]	1: IIC_WRREG access is possible. 0: IIC_WRREG access is impossible. (def)	
				[7]	1: Under a picture output 0: Picture output end (def)	
3-6	Video signal polarity	94h [25dw]	R/W	SIG_POLARITY[2:0]		
				[0]	0:VS assert L (def) 1:VS assert H	
				[1]	0:HS assert L 1:HS assert H (def)	
				[2]	0:DOE assert L 1:DOE assert H (def)	

No.	Register name	Addr [8:0]	R/W	Bit field		Functions
3-7	MIRQ	98h [26dw]	R	MIRQ_REG[7:0]		1 is set up, when 1 is set as the register to which Bit 4-7 corresponds and the event of each register occurs. It will be cleared if a register is read.
				[0]	1: Set at the time of a capture / display start. 0: Waiting for an event (def)	
				[1]	1: Set at the time of a capture / display end. 0: Waiting for an event (def)	
				[2]	1: Set at the time of compression / de-compression start. 0: Waiting for an event (def)	
				[3]	1:Set at the time of compression N – 1/ de-compression start 0: Waiting for an event (def)	
			R/W	[4]	1:Bit0 enable 0:Bit0 read as 0 (def)	
				[5]	1:Bit1 enable 0:Bit1 read as 0 (def)	
				[6]	1:Bit2 enable 0:Bit2 read as 0 (def)	
				[7]	1:Bit3 enable 0:Bit3 read as 0 (def)	
3-8	H_START	9Ch [27dw]	R/W	HSTART[9:0]		Set up in consideration of the pair of U and V. H_START is united with the position of U.
				[9:0]	78h: = 120 (def) Nh : Picture data horizontal start position	
3-9	V_START	A0h [28dw]	R/W	VSTART[9:0]		Unite with the start line position of the first field at interlace.
				[9:0]	11h: = 17(def) Nh : Picture data vertical start position	
3-10	H_COUNT	A4h [29dw]	R/W	HCOUNT[9:0]		Set up in consideration of the pair of U and V. Must be the multiple of 2.
				[9:0]	280h: = 640 (def) Nh : The number of picture data horizontal effective pixels	
3-11	V_COUNT	A8h [2Adw]	R/W	VCOUNT[9:0]		Must be the multiple of 2 at interlace mode.
				[9:0]	1E0h: = 480 (def) Nh: The number of picture data vertical effective lines	
3-12	R_XBASE	ACh [2Bdw]	R/W	R_XBASE[9:0]		N is specified by the integral multiple of 2.
				[9:0]	0h: (def) Nh : SDRAM storing domain horizontal start position specification of a capture and display data	
3-13	R_YBASE	B0h [2Cdw]	R/W	R_YBASE[9:0]		N is specified by the integral multiple of 2.
				[9:0]	0h: (def) Nh : SDRAM storing domain vertical start position specification of a capture and display data	
3-14	R_XRANGE	B4h [2Ddw]	R/W	R_XRANGE[9:0]		M is specified by the integral multiple of 16.
				[9:0]	280h: =640 (def) Mh : SDRAM storing domain horizontal range specification of a capture and display data	
3-15	R_YRANGE	B8h [2Edw]	R/W	R_YRANGE[9:0]		M is specified by the integral multiple of 8.
				[9:0]	1E0h: = 480 (def) Mh : SDRAM storing domain vertical range specification of a capture and display data	

No.	Register name	Addr [8:0]	R/W	Bit field		Functions
3-16	B_XBASE	BCh [2Fdw]	R/W	B_XBASE[9:0]		N is specified by the integral multiple of 2.
				[9:0]	0h: (def) Nh: SDRAM storing domain horizontal start position specification of compression and de-compression data	
3-17	B_YBASE	C0h [30dw]	R/W	B_YBASE[9:0]		N is specified by the integral multiple of 2.
				[9:0]	0h: (def) Nh: SDRAM storing domain vertical start position specification of compression and de-compression data	
3-18	B_XRANGE	C4h [31dw]	R/W	B_XRANGE[9:0]		M is specified by the integral multiple of 16. set as de-compressed image size.
				[9:0]	280h: = 640 (def) Mh: SDRAM storing domain horizontal range specification of compression and de-compression data	
3-19	B_YRANGE	C8h [32dw]	R/W	B_YRANGE [9:0]		M is specified by the integral multiple of 8. set as de-compressed image size.
				[9:0]	1E0h: = 480 (def) Mh: SDRAM storing domain vertical range specification of compression and de-compression data	
3-20	R_SAMPLIN G	CCh [33dw]	R/W	R_SAMPLING[0]		Used when capture the QVGA image sub-sampled from VGA image
				[0]	1: x1/4 sub-smpling 0: no sub-sampling (def)	

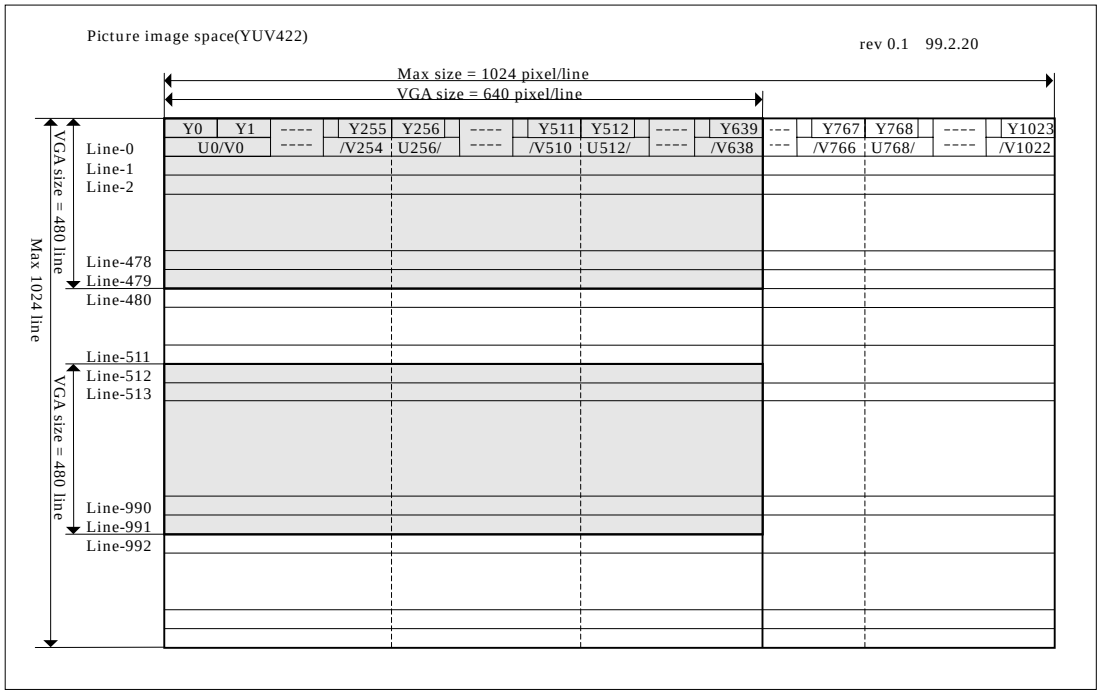
No.	Register name	Addr [8:0]	R/W	Bit field		The setup at LSI use	
				VRJ SR_addr [bit width]	default – meaning	Compression	De-compression
4	VRJ register (refer to the KL5A71007 JPEG chip datasheet for more details)						
4-1	Bus mode	100h [40dw]	R/W	SR_h00[3:0]	0h - 8bit bus	5h	
4-2	Signal active level	108h [42dw]	R/W	SR_h02[4:0]	1Fh – req/ack asrtH	1Fh	
4-3	PDAT use	110h [44dw]	R/W	SR_h04[0]	0b - pdat unused	1b	
4-4	Mode specify	118h [46dw]	R/W	SR_h06[6:0]	00h – reg acc,comp	3Fh	3Eh
4-5	Limit of compressed data volume (kBytes)	120h [48dw]	R/W	SR_h08[7:0] (LoB)	0000h – comp data volume unlimited	FFFFh	--
		124h [49dw]	R/W	SR_h09[7:0] (HiB)			
4-6	Compressed data format	128h [4Adw]	R/W	SR_h0A[3:0]	Ch – code with header table	-- (unchanged)	--
4-7	Table data	140h [50dw]	W	SR_h10[15:0]	Write only reg Use table setting	Must be setup the table data before compression	--
4-8	Restart interval	148h [52dw]	R/W	SR_h12[7:0] (LoB)	0000h – no RST code generated	-- (unchanged)	--
		14Ch [53dw]	R/W	SR_h13[7:0] (HiB)			
4-9	Number of lines	150h [54dw]	R/W	SR_h14[7:0] (LoB)	0000h – must be set the number of lines (compression)	1E0h (VGA) 0F0h(QVGA)	--
		154h [55dw]	R/W	SR_h15[7:0] (HiB)			
4-10	Number of pixels	158h [56dw]	R/W	SR_h16[7:0] (LoB)	0001h – must be set the number of pixels (compression)	280h (VGA) 140h(QVGA)	--
		15Ch [57dw]	R/W	SR_h17[7:0] (HiB)			
4-11	Number of component	160h [58dw]	R/W	SR_h18[5:0]	9h – must be set Nf and Ns (comp.)	1Bh (YUV422)	--
4-12	Information of 1st component SOF	168h [5Adw]	R/W	SR_h1A[7:0]	0500h – must be set the SOF param (compression)	0601h(Y-compo)	--
		16Ch [5Bdw]	R/W	SR_h1B[5:0]			
4-13	Information of 2nd component SOF	170h [5Cdw]	R/W	SR_h1C[7:0]	0501h – must be set the SOF param (compression)	1502h(U-compo)	--
		174h [5Ddw]	R/W	SR_h1D[5:0]			
4-14	Information of 3rd component SOF	178h [5Edw]	R/W	SR_h1E[7:0]	0502h - must be set the SOF param (compression)	1503h(V-compo)	--
		17Ch [5Fdw]	R/W	SR_h1F[5:0]			
4-15	Information of 4th component SOF	180h [60dw]	R/W	SR_h20[7:0]	0503h - must be set the SOF param (compression)	--	--
		184h [61dw]	R/W	SR_h21[5:0]			
4-16	Component information SOS	188h [62dw]	R/W	SR_h22[7:0]	3210h - must be set the SOS param (compression)	0ED0h	--
		18Ch [63dw]	R/W	SR_h23[7:0]			

No.	Register name	Addr [8:0]	R/W	Bit field		The setup at LSI use	
				VRJ SR_addr [bit width]	default – meaning	Compression	De-compression
4	VRJ register (refer to the KL5A71007 JPEG chip datasheet for more details)						
4-17	VRJ soft-reset	190h [64dw]	R/W	SR_h24[0]	0b	Set 1b before processing	
4-18	Start command	1A0h [68dw]	R/W	SR_h28[0]	0b	Use when direct processing of JPEG	
4-19	End command	1A8h [6Adw]	R/W	SR_h2A[0]	0b	Use when direct processing of JPEG	
4-20	Compressed data	1B0h [6Cdw]	R/W	VRJ SR_h2C[15:0]	- must be check status register before acccess	Use when direct processing of JPEG	
4-21	Pixel data	1B8h [6Edw]	R/W	SR_h2E[15:0]	- must be check status register before acccess	Use when direct processing of JPEG	
4-22	Status	1C0h [70dw]	R	SR_h30[3:0]	0h	Use when direct processing of JPEG	
4-23	IRQ flag	1C8h [72dw]	R	SR_h32[3:0]	0h	Read when VRJ IRQ assert	
			R/W	SR_h32[7:4]	0h	Ah (assert IRQ when end of processand error. Cleared automatically by HIC)	
4-24	Compressed data volume (kBytes)	1D0h [74dw]	R/W	SR_h34[7:0] (LoB)	0000h	Read if needed. Read only.	--
		1D4h [75dw]	R/W	SR_h35[7:0] (HiB)			
4-25	Error report	1D8h [76dw]	R	SR_h36[7:0]	00h (no error)	Use when direct processing of JPEG	
4-26	Test register	1F4h [7Ddw]	R/W	SR_h3D[7:0]	?	Use only for test. Never access in normal operation.	

12.3 Frame Memory Mapping and Main Memory access method

Correspondence of picture image space and the physical address space of a frame memory is explained. The relation of Y / C component and a line in the picture image space of 1,024 pixel x 1,024 line was shown in figure 12.3.1.

Figure 12.3.1 picture image space and Y/C component and line



This picture image space is linearly mapped to SDRAM used for a frame memory. Although two VGA domains is used by changing at continuation processing etc., as for these VGA domains are mapped to (0, 0) to (639,479) and (0,512) to (639,991) as (Y-component, Line). Moreover, default domain used for the capture, the display, etc. of a still picture is (0, 0) to (639,479).

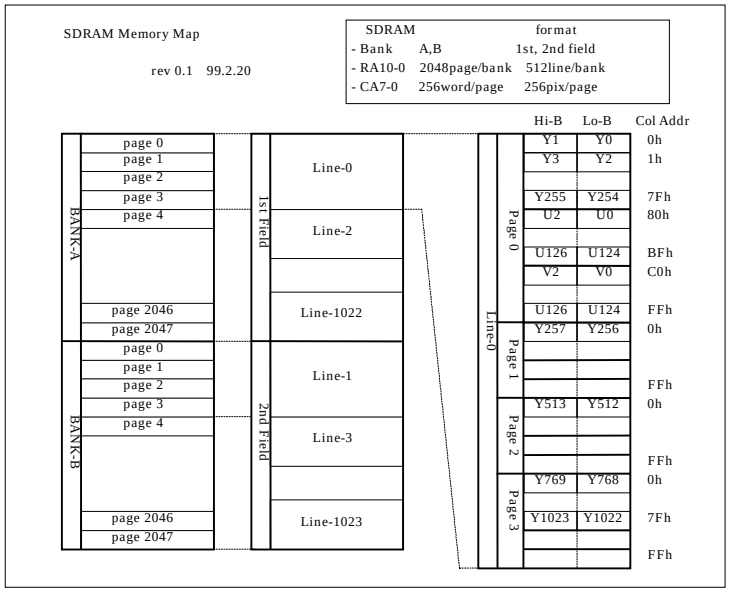
Parameter of MCC used for memory domain specification, XBASE, YBASE, XRANGE and YRANGE are set up as the above-mentioned picture image space (Y-component, Line) and the range.

Physical mapping to a frame memory was shown in the figure 12.3.2.

16Mb(1M x 16b) SDRAM used for a frame memory was two bank composition, the first field (Line-0,2,4, …) is arranged to the bank A, and the second field (Line-1,3,5, …) to bank B. This scheme is the same also at the time of progressive.

The YUV component storing domain for 256 pixels is mapped to each page of SDRAM, and 1,024 pixels one line is assigned by continuous 4 pages.

Figure 12.3.2 SDRAM memory map



When read/write directly to a frame memory, the value set as R_XBASE and the R_YBASE parameter is mapped to the bank of SDRAM, page No, and a WORD address as follows and access to the SDRAM. At the time of continuation direct access, a memory address is increased linearly.

Be careful since not correspond to coordinates (Y-component and Line) in picture image space simply.

BANK_A for R_YBASE[9] == 0

BANK B for R_YBASE[9] == 1

ROW Addr (page No) == {R_YBASE[8:0],R_XBASE[9:8]} // 0 to 2047

COL Addr (word addr) == R_XBASE[7:0] // 0 to 255

12.4 Main Memory access method

The access method to the main memory in PCI master mode in continuous capture & compression, a continuous de-compression & display and a continuous picture output was shown below.

In the case of continuous compression / picture output

1) Build a page table (256 entries) on a main memory externally.

2) Set the storing address of a page table to a PT_ADDR register.

3) Start a continuous command.

4) LSI specifies the entry of a PT_ADDR register, reads the entry address of a page table inmaster mode, and reads the base address of the page which should transmit output data.

5) LSI writes generated output data in master mode to the page of an entry.

6) If a page fills, the page of the following entry will be accessed in the procedure of the above 4 and 5.

7) If it finishes outputting data for one frame, the entry information and the amount of data of last page will be recorded to FIR register.

8) LSI waits for a data output until a program will release the page of a pre-frame and an entry will newly become applicable, if entries run short before finishing outputting data for one frame.

9) Although the number of entries is 256 pieces (1MByte) at a continuous picture output and 1,024 pieces (4 M bytes) at continuous compression, the entry is as ring buffer form and the domain of one frame which can be maximum used corresponds to all entries.

10) When the program has recognized that the output of one frame finished, it transmits data on a main memory to external Storage etc., and it releases an entry.

In the case of continuous de-compression

1) Build a page table (256 entries) on a main memory externally.

2) Set the storing address of a page table to a PT_ADDR register.

3) Prepare compression data which should be de-compress for a page.

4) A program sets up the entry information of a frame which was ready and the amount of data of the last page in FIR register.

5) Start a continuation command.

6) LSI specifies the entry of a PT_ADDR register and reads the base address of the page which should input compression data in master mode.

7) LSI reads input data which should be de-compress from the page of an entry in master mode.

8) If a page fills, the page of the following entry will be accessed in the procedure of the above 6 and 7.

9) If it finishes inputting data for one frame, the needlessness of frame information will be set to FIR register.

10) When processing of the set-up frame is completed and data of the following frame is not prepared, wait for data preparation is finished.

11) The number of entries is 256 pieces (1MByte).

Figure 12.4.1 Main memory access method at continuous compression/de-compression

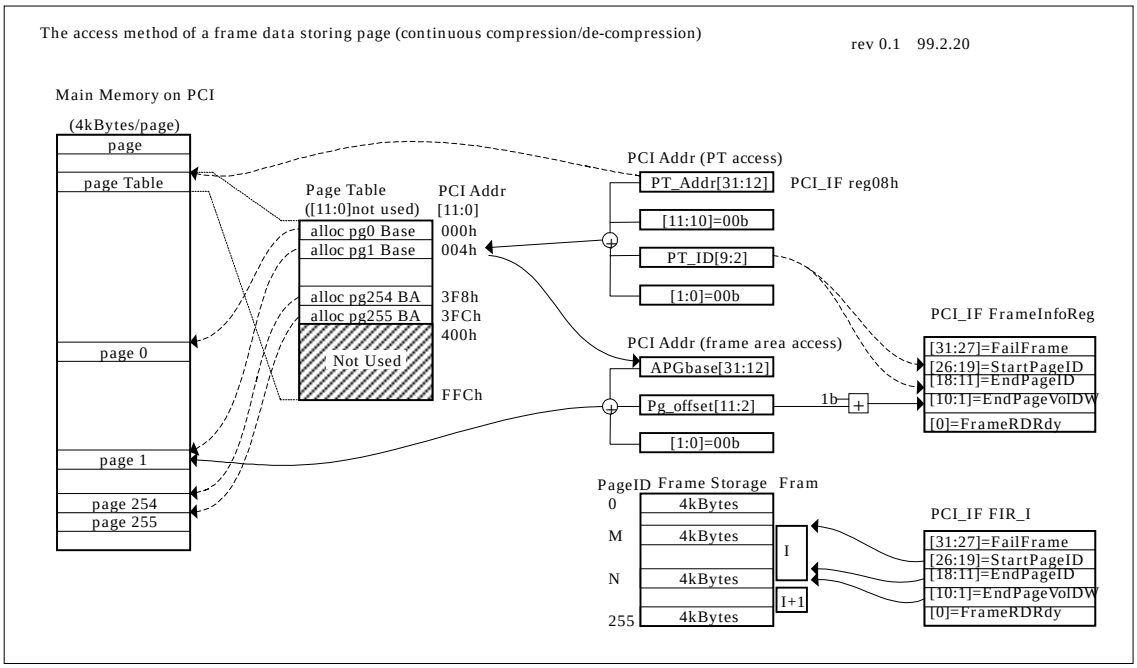
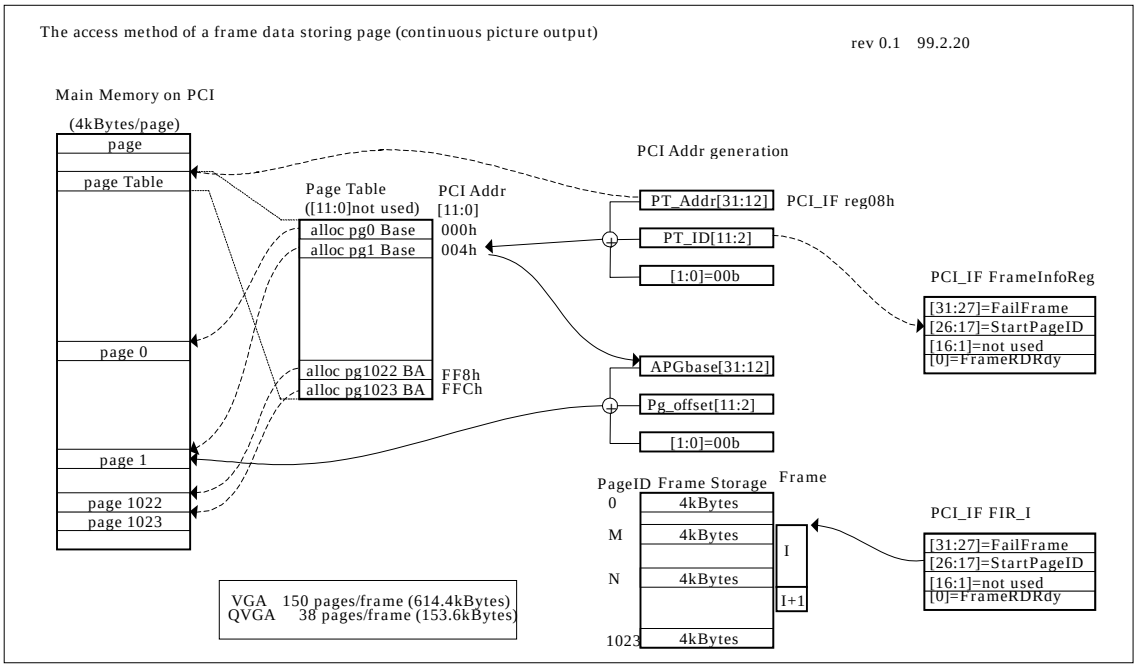


Figure 12.4.2 Main memory access method at continuous picture output

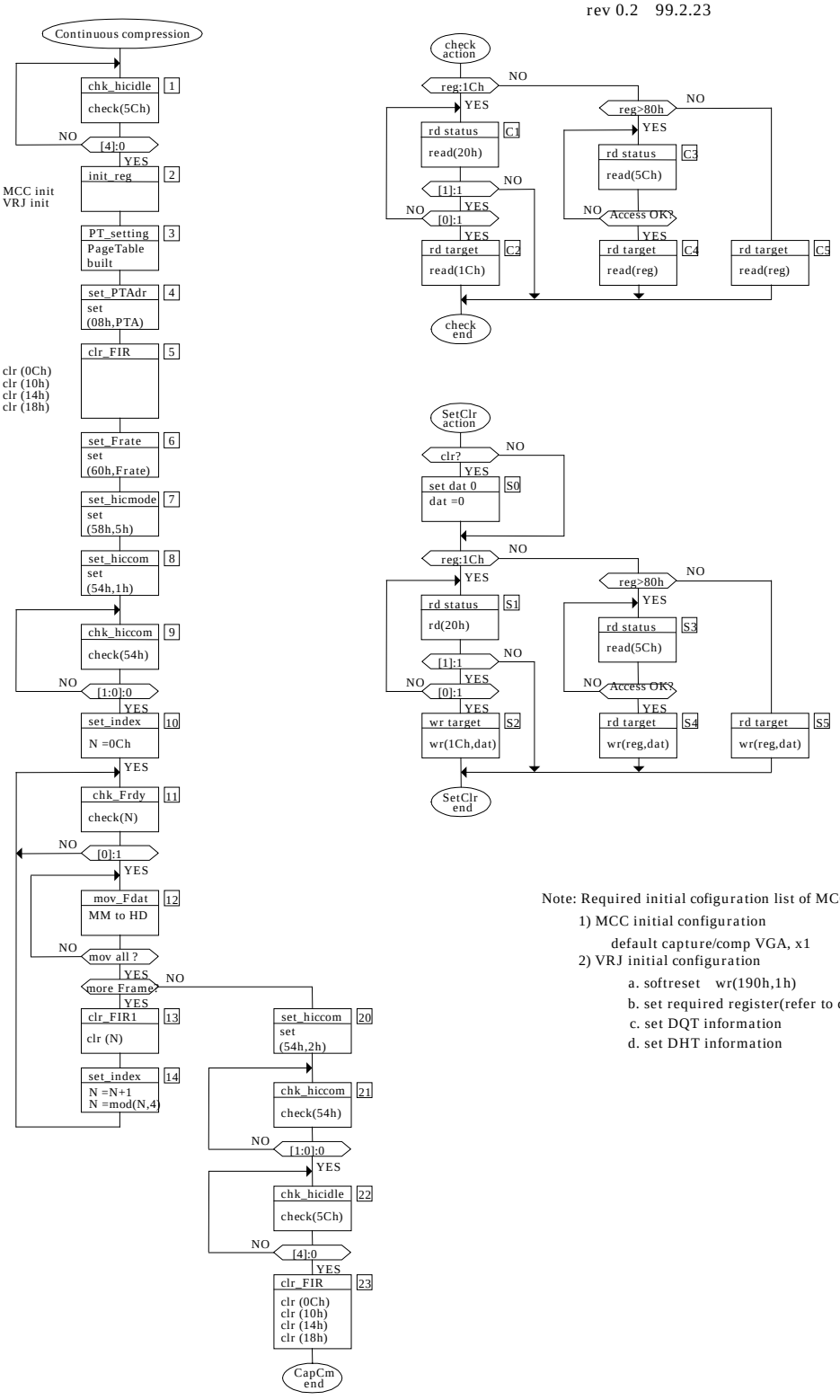


13. Device control flow

The control procedure of continuous compression is shown below as an example of a control flow.

Continuous compression control procedure (Host PC)

rev 0.2 99.2.23



Note: Required initial cofiguration list of MCC/VRJ

1) MCC initial configuration
   default capture/comp VGA, x1
2) VRJ initial configuration
   a. softreset wr(190h,1h)
   b. set required register(refer to datasheet)
   c. set DQT information
   d. set DHT information

14. The example of an initial cofiguration

The example of an initial cofiguration of the internal register in each mode of operation is shown below.

14.1 Through Picture Display

The initial cofiguration of Video codec is set by PCI Target write-mode.

```
[Procedure]   1. TGT write  (20dw,1h);          // MCC setting start command
              2. loop until all data write
                   2a. TGT read  (24dw);              // A check of MCC status
                       if [6] == 1b goto 2b;
                       else          goto 2a;
                   2b.                                // Writing of initial cofiguration data
                       TGT write (21dw, write_data[7:0]);
              3. TGT write (20dw, 2h);           // MCC setting end command
```

14.2 Frame Memory Direct Writing

Frame memory writing is performed in PCI Target write-mode.

```
[Procedure]   1. TGT read  (24dw);                     // A check of MCC status
                  if [7:0] == 00h goto 2;
                  else TGT write (20dw,Fh)         // MCC soft-reset
                       goto 1;
              2. TGT write (2Bdw,start_Xbase);   // set the R_XBASE of MCC
              3. TGT write (2Cdw,start_Ybase);   // set the R_YBASE of MCC
              4. TGT write (20dw,3h);            // set the FM write command to MCC
              5. loop until all data write
                   5a. TGT read  (24dw);          // A check of MCC status
                       if [4] == 1b goto 5b;
                       else          goto 5a;
                   5b.                                // FM write word data
                       TGT write (22dw, write_data[15:0]);
              6. TGT write (20dw,5h);          // set the FM access stop command to MCC
```

14.3 Frame Memory Direct Read-out

Frame memory read-out is performed by PCI Target read mode.

[Procedure] 1. // check the MCC status (same as 14.2.1)

2. TGT write (2Bdw,start_Xbase); // set the R_XBASE of MCC

3. TGT write (2Cdw,start_Ybase); // set the R_YBASE of MCC

4. TGT write (20dw,4h); // set the FM read-out command to MCC

5. loop until all data write

5a. TGT read (24dw); // check the MCC status

if [5] == 1b goto 5b;

else goto 5a;

5b. TGT read (23dw); // FM read word data

read_data low word [15:0] is valid

6. TGT write (20dw,5h); // set the stop FM access command to MCC

14.4 Still image capture

Capture the picture data inputted from Video Bus to a frame memory.

[Procedure] 1. // check the MCC status (same as 14.2.1)

2. // set the polarity of DOE, HS, VS – not needed to set if use default value

TGT write (25dw,write_data[2:0]); // set the SIG_POLARITY of MCC

3. // set the Video Bus picture data valid range -- not needed to set if use default value

TGT write (27dw,write_data[9:0]); // set the H_START of MCC

TGT write (28dw,write_data[9:0]); // set the V_START of MCC

TGT write (29dw,write_data[9:0]); // set the H_COUNT of MCC

TGT write (2Adw,write_data[9:0]); // set the V_COUNT of MCC

4. // set the frame memory storing domain -- not needed to set if use default value

TGT write (2Bdw,write_data[9:0]); // set the R_XBASE of MCC

TGT write (2Cdw,write_data[9:0]); // set the R_YBASE of MCC

TGT write (2Ddw,write_data[9:0]); // set the R_XRANGE of MCC

TGT write (2Edw,write_data[9:0]); // set the R_YRANGE of MCC

5. // set the sub-sampling at capturing -- not needed to set if use default value

TGT write (33dw,write_data[0]); // set the R_SAMPLING of MCC

6. TGT write (16dw,1h); // set the still image capture to HIC mode

7. TGT write (15dw,1h); // HIC processing start is directed.

8. Monitor the end of still picture capture processing by the polling of HIC status, or IRQ assert (it is initial cofiguration necessity beforehand) of PCI IF.

14.5 Display

The picture data recorded to the frame memory is outputted to Video Bus for display.

[Procedure] 1. // check the MCC status (same as 14.2.1)

2. // set the polarity of DOE, HS, VS – not needed to set if use default value

3. // set the Video Bus picture data valid range -- not needed to set if use default value

4. // set the frame memory storing domain -- not needed to set if use default value

5. TGT write (16dw,2h); // set the display to HIC mode

6. TGT write (15dw,1h); // HIC processing start is directed.

7. // An end command is set up at the display end.

TGT write (15dw,2h); // HIC processing end is directed.

14.6 Still image compression

Picture data recorded to the frame memory is compressed and outputted to a PCI bus.

[Procedure] 1. // This setup is performed if it is PCI Target access.

TGT write (00dw,3h); // set the PCI_MODE of PCI IF

2. // set the frame memory storing domain -- not needed to set if use default value

TGT write (2Fdw,write_data[9:0]); // set the B_XBASE of MCC

TGT write (30dw,write_data[9:0]); // set the B_YBASE of MCC

TGT write (31dw,write_data[9:0]); // set the B_XRANGE of MCC

TGT write (32dw,write_data[9:0]); // set the B_YRANGE of MCC

3. // initial setup of VRJ

//The required item of a VRJ register (see No. 4 of the table of 12.2) is set up by TGT write.

4. // A quantization table is set to VRJ.

Detailed abbreviation

5. // A Huffman table is set to VRJ

Detailed abbreviation

6. // set the IRQ of HIC

TGT write (1dw,200h); // set the enable of VRJ IRQ

7. // set the address pointer of page table (only in PCI Master mode)

TGT write (2dw,write_data[31:0]); // set the PT_ADDR of PCI IF

8. TGT write (16dw,3h); // set the still image compression to HIC mode

9. TGT write (15dw,1h); // HIC processing start is directed.

15. Electrical Caracteristics

15.1 Electric Caracteristics (1)

The absolute maximum rating, the recommended operating conditions, DC characteristic and input/output terminal capacitance of LSI are shown.

Figure 15.1.1 absolute maximum rating

No.	Parameter	Symbol	Limit	Unit
1	Supply voltage	Vdd	-0.3 - +3.8	V
2	Input voltage	Vin	-0.3 - +5.6	V
3	Output current	Iout	± 30	mA
4	Storage temperature	Tstg	-55 - +125	°C

Figure 15.1.2 Recommended operatng conditions

No.	Parameter	Symbol	Limit	Unit
5	Supply voltage	Vdd	+3.0 - +3.6	V
6	Operating ambient temperature	Ta	0 - +85	°C

Figure 15.1.3A DC caracteristics (1) (under recommended operating condition) – except PCI buffer

No.	Parameter	Symbol	conditions	Min.	Max.	unit
7A	Low level input voltage	Vil		--	0.8	V
8A	High level input voltage	Vih		2.0	--	V
9A	Low level output voltage	Vol	Iol = +4mA	--	0.4	V
10A	High level output voltage	Voh	Ioh = -4mA	2.4	--	V
11A	Input leakage current (low)	Iil	Vin = GND	-10	--	µA
12A	Input leakage current (high)	Iih	Vin = Vdd	--	+10	µA

Figure 15.1.3B DC caracteristics (1) (under recommended operating condition)– PCI buffer

No.	Parameter	Symbol	conditions	Min.	Max.	unit
7B	Low level input voltage	Vil		-0.3	0.3Vdd	V
8B	High level input voltage	Vih		0.5Vdd	5.25	V
9B	Low level output voltage	Vol	Iol = +1.5mA	--	0.1Vdd	V
10B	High level output voltage	Voh	Ioh = -0.5mA	0.9Vdd	--	V
11B	Input leakage current (low)	Iil	Vin = GND	-10	--	µA
12B	Input leakage current (high)	Iih	Vin = Vdd	--	+10	µA

Figure 15.1.4 DC caracteristics (2) (under recommended operating condition)

No.	Parameter	Symbol	Condition	Min.	Max.	unit
13	3-state leakage current	Ioz	3-state output Vnode= Vdd or GND	-10	+10	µA
14	Standby current	Ids	All input pins = Vdd/GND All output pins = open MCORE_RDY = L (LED off)	--	500?	µA
15	Lowpower current	Idlp	MCORE is LOWPOWER PCI IF is idle SYSCLK,CLK=33MHz Other inputs = Vdd/GND Output = Vdd/GND/3-state MCORE_RDY = L (LED off)	--	2?	mA
16	Operating supply current	Idop	Continuous compression (Cload = 30pF) MCORE_RDY : Ioh=-6mA	--	160?	mA
17	Supply current at idle	Inop	No-operation (NOOP) Input = 10MHz, CLK = 33MHz Output =Vdd/GND/3-state MCORE_RDY : Ioh=-6mA	--	130?	mA
18	Input capacitance	Cin	f=1MHz, Vin=GND, vin=100 mVrms	--	10	pF
19	Output capacitance	Cout		--	10	pF

Figure 15.1.5 PCI buffer AC caracteristics (under recommended operating condition)

No.	Parameter	Symbol	Condition	Min.	Max.	unit
18	Switching L output current	Iol(AC)	Vdd>Vout=>0.6Vdd	16Vdd	--	mA
			0.6Vdd>Vout>0.1Vdd	26.7Vout	--	mA
			0.18Vdd>Vout>0	--	*Eq-A	mA
	(test point)		Vout=0.18Vdd	--	38Vdd	mA
19	Switching H output current	Ioh(AC)	0<Vout<=0.3Vdd	12Vdd	--	mA
			0.3Vdd<Vout<0.9Vdd	-17.1* (Vdd-Vout)	--	mA
			0.7Vdd<Vout<Vdd	--	*Eq-B	mA
	(test point)		Vout=0.7Vdd	--	-32Vdd	mA
20	Output rising through rate	Tr	0.2Vdd → 0.6Vdd	1	4	V/ns
21	Output falling through rate	Tf	0.6Vdd → 0.2Vdd	1	4	V/ns

Note: Equation-A: Iol(AC)=(256/Vdd)*Vout*(Vdd-Vout) for 0.18Vdd>Vout>0

Equation-B: Ioh(AC)=(98/Vdd)*(Vout-Vdd)*(Vout+0.4Vdd) for 0.7Vdd<Vout<Vdd

15.2 Electric Caracteristics (2)

15.2.1 Video Bus (ZV-port) AC Timing

AC caracteristics of Video Bus at ZV-port mode

Figure 15.2.1.1 Video Bus (ZV-port) AC timing 1

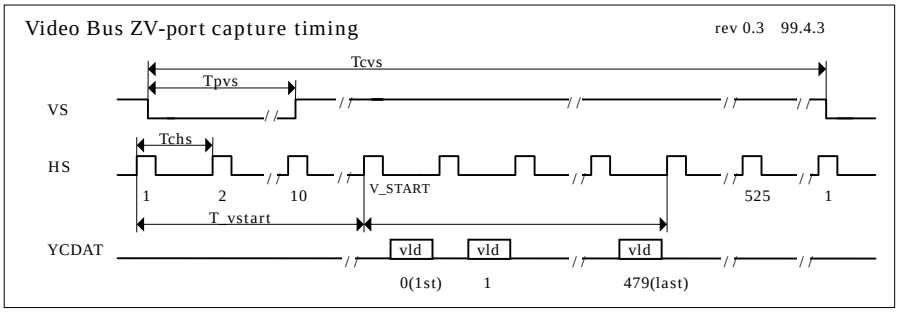


Table 15.2.1.1 Video Bus (ZV-port) AC timing 1

No.	Symbol	Parameter	Min.	Typ.	Max.	unit	Note
1	Tcvs	VS cycle time	--	525	--	Ths	29.97Hz
2	Tpvs	VS low pulse width	--	9	--	Ths	
3	Tchs	HS cycle time	--	910	--	Tpck	15.735kHz (63.55 us)
4	T_vstart	Valid data start position	--	V_START - 1	--	Ths	Register setting (def : 17Ths)
5	T_vcount	Valid data line count	--	V_COUNT	--	Tvs	Register setting (def : 480Tvs)

Figure 15.2.1.2 Video Bus (ZV-port) AC timing 2

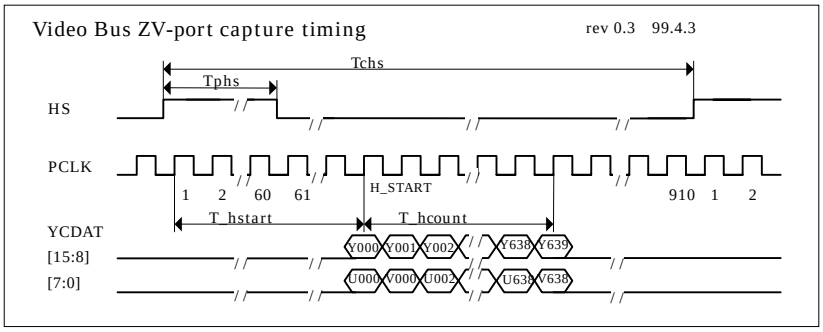


Table 15.2.1.2 Video Bus (ZV-port) AC timing 2

No.	Symbol	Parameter	Min.	Typ.	Max.	unit	Note
1	Tchs	HS cycle time	--	910	--	Tpck	15.735kHz
2	Tphs	HS low pulse width	--	60	--	Tpck	
3	T_hstart	Valid data start position	--	H_START	--	Tpck	Register setting (def : 120Tpck)
4	T_hcount	Valid data pixel count	--	H_COUNT	--	Tpck	Register setting (def : 640Tpck)

Figure 15.2.1.3 Video Bus (ZV-port) AC timing 3

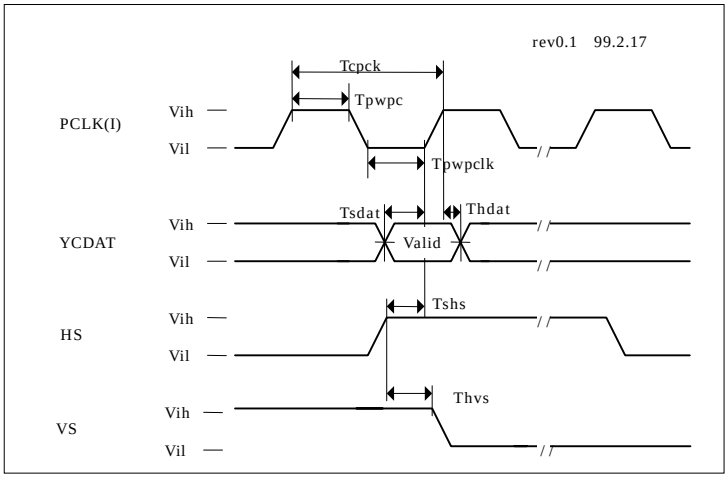


Table 15.2.1.3 Video Bus (ZV-port) AC timing 3

No.	Symbol	Parameter	Min.	Typ.	Max.	unit	Note
1	Tcpck	PCLK cycle time	--	69.85	--	ns	14.318MHz
2	Tpwpck	PCLK pulse width	28	--	42	ns	
3	Tsdat	YCDAT setup to PCLK	20	--	--	ns	
4	Thdat	YCDAT hold from PCLK	5	--	--	ns	
5	Tshs	HS setup to PCLK	20	--	--	ns	
6	Thvs	VS hold from HS	10	--	--	ns	

15.2.2 Video Bus (Digital YC) AC timing

AC caracteristics of Video Bus at Digital YC mode

Figure 15.2.2.1 Video Bus (Digital YC) AC timing 1

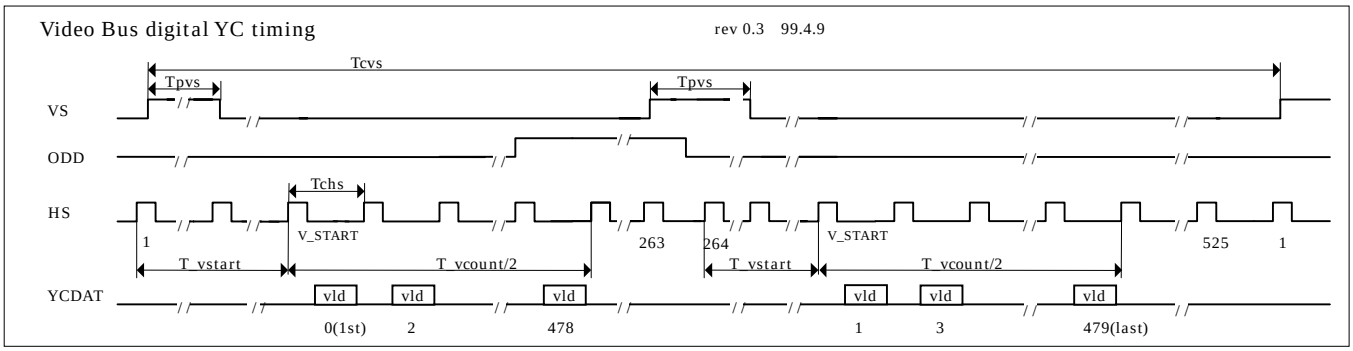


Table 15.2.2.1 Video Bus (Digital YC) AC timing 1

No.	Symbol	Parameter	Min.	Typ.	Max.	unit	Note
1	Tcvs	VS cycle time	--	525	--	Ths	29.97Hz
2	Tpvs	VS low pulse width	--	9	--	Ths	
3	Tchs	HS cycle time	--	780	--	Tpck	15.735kHz (63.55 us)
4	T_vstart	Valid data start position	--	(V_START – 1)/2	--	Ths	Register setting (def : 17Ths)
5	T_vcount	Valid data line count	--	V_COUNT	--	Tvs	Register setting (def : 480Tvs)

Figure 15.2.2.2 Video Bus (Digital YC) AC timing 2

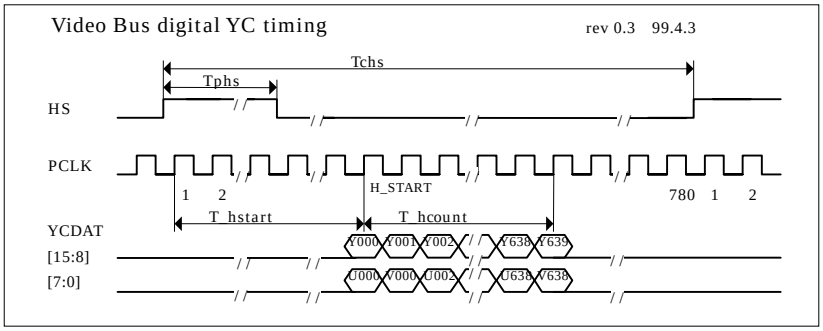


Table 15.2.2.2 Video Bus (Digital YC) AC timing 2

No.	Symbol	Parameter	Min.	Typ.	Max.	unit	Note
2-1	Tchs	HS cycle time	--	780	--	Tpck	15.735kHz (63.5us)
2-2	Tphs	HS low pulse width	--	64	--	Tpck	
2-3	T_hstart	Valid data start position	--	H_START - 1	--	Tpck	Register setting (def : 120Tpck)
2-4	T_hcount	Valid data pixel count	--	H_COUNT	--	Tpck	Register setting (def : 640Tpck)

Figure 15.2.2.3 Video Bus (Digital YC) AC timing 3 (input)

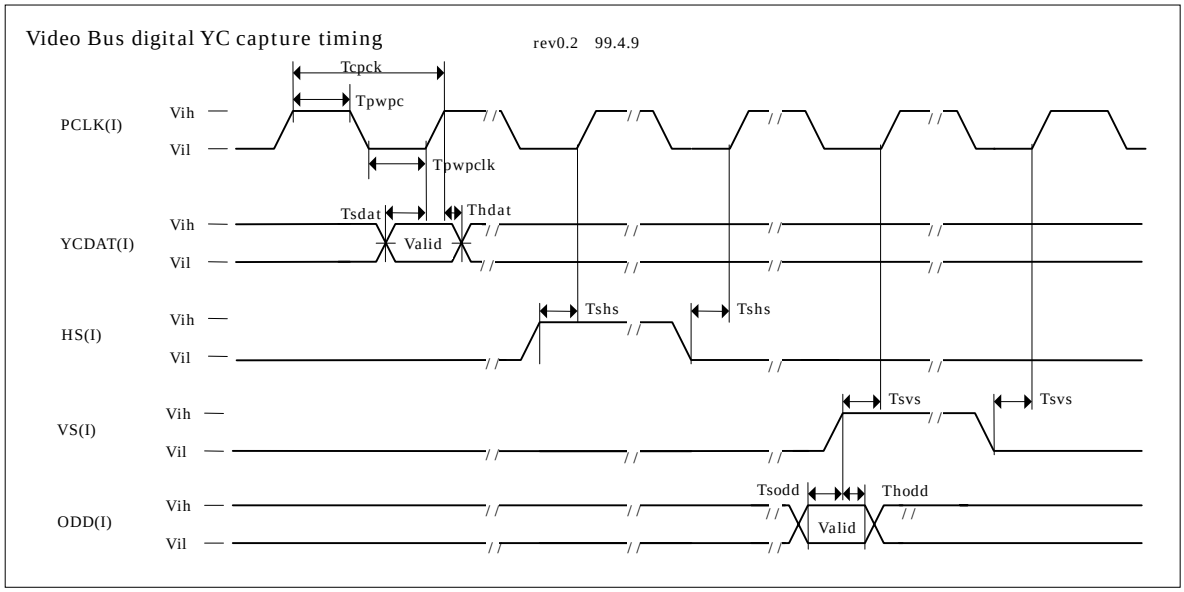


Table 15.2.1.3 Video Bus (Digital YC) AC timing 3 (input)

No.	Symbol	Parameter	Min.	Typ.	Max.	unit	Note
1	Tcpck	PCLK cycle time	--	81.5	--	ns	12.27MHz
2	Tpwpck	PCLK pulse width	32	--	49	ns	
3	Tsdat	YCDAT setup to PCLK	20	--	--	ns	
4	Thdat	YCDAT hold from PCLK	5	--	--	ns	
5	Tshs	HS setup to PCLK	20	--	--	ns	
6	Tsvs	VS setup to PCLK	20	--	--	ns	
7	Tsodd	ODD setup to VS	1	--	--	Ths	1Ths=63.5us
8	Thodd	ODD hold from VS	1	--	--	Ths	1Ths=63.5us

Figure 15.2.2.4 Video Bus (Digital YC) AC timing 4 (output)

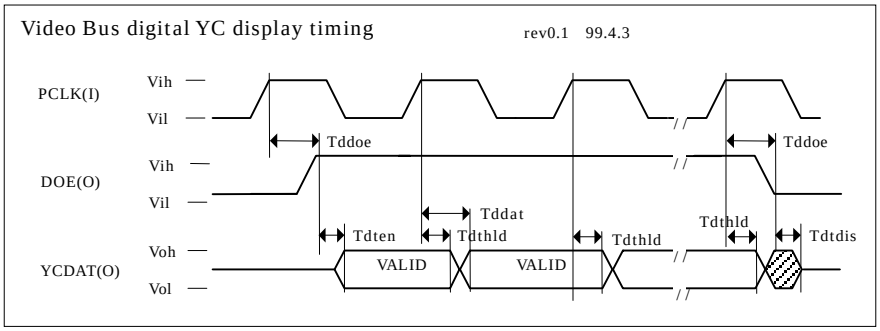


Table 15.2.1.4 Video Bus (Digital YC) AC timing 4 (output)

No.	Symbol	Parameter	Min.	Typ.	Max.	unit	Note
1	Tddoe	DOE output delay	5	--	20	ns	Output load = 30pF
2	Tdten	YCDAT output delay (DOE)	0	--	10	ns	Output load = 30pF
3	Tdthld	YCDAT valid hold time	5	--	--	ns	Output load = 30pF
4	Tddat	YCDAT output delay	5	--	20	ns	Output load = 30pF
5	Tdtdis	YCDAT disable delay (DOE)	0	--	10	ns	Output load = 30pF

15.2.3 Mem Bus AC timing

AC caracteristics of Memory Bus

Figure 15.2.3.1 Memory Bus AC timing

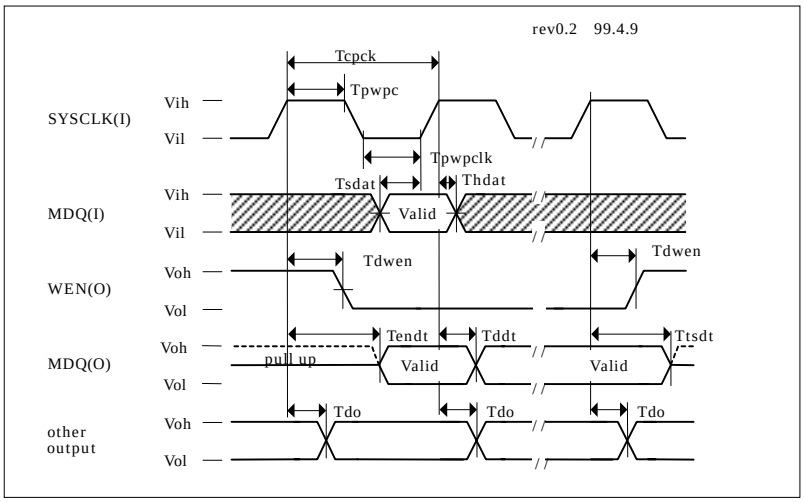


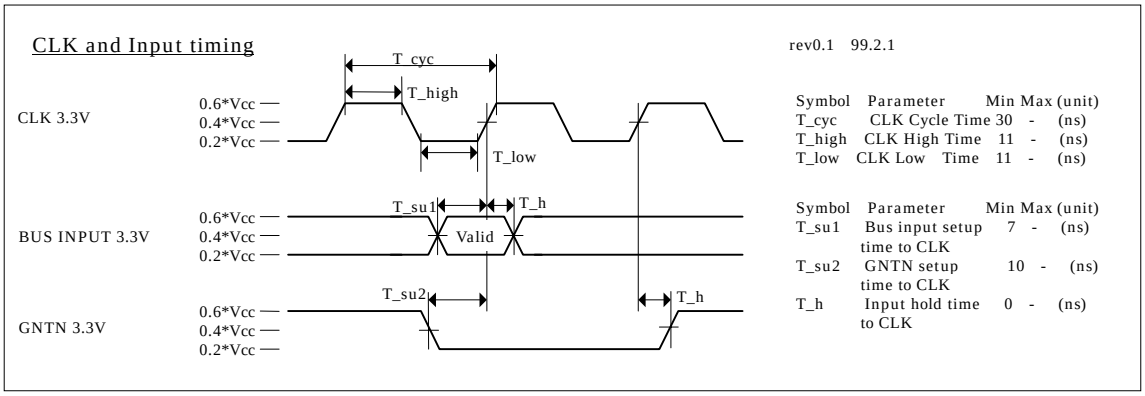
Table 15.2.3.1 Memory Bus AC timing

No.	Symbol	Parameter	Min.	Typ.	Max.	unit	Note
1	Tcpck	SYSCLK cycle time	--	30	--	ns	33MHz (same phase with CLK of SDRAM)
2	Tpwpck	SYSCLK pulse width	12	--	18	ns	
3	Tsdat	MDQ input set-up time	10	--	--	ns	
4	Thdat	MDQ input hold time	0	--	--	ns	
5	Tdwen	MWEN output delay	--	--	16	ns	Output load = 30pF
6	Tendt	MDQ output enable time	--	--	20	ns	Output load = 30pF
7	Ttsdt	MDQ output disable time	--	--	22	ns	Output load = 30pF
8	Tddt	MDQ output delay	--	--	18	ns	Output load = 30pF
9	Tdo	Output delay except MDQ	--	--	16	ns	Output load = 30pF

15.2.4 PCI Bus AC timing

AC caracteristics of PCI Bus

Figure 15.2.4.1 PCI Bus AC timing (input)

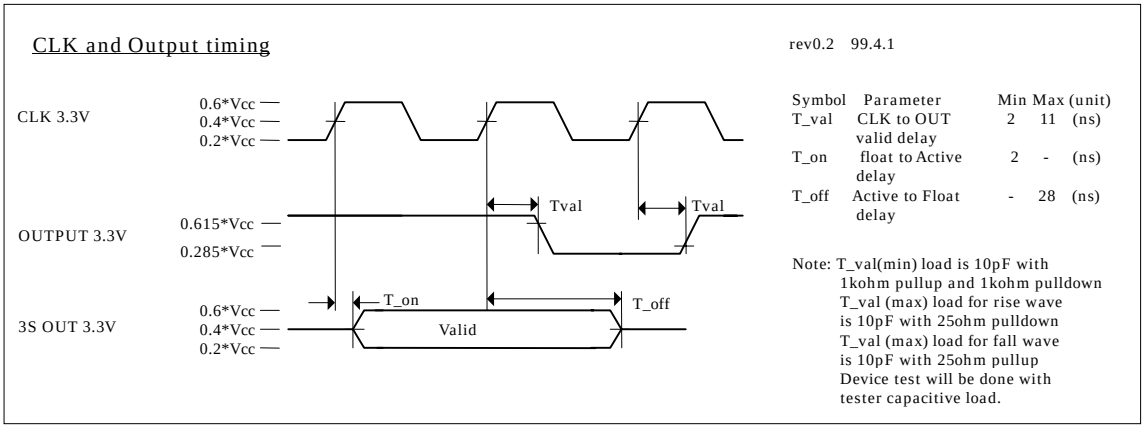


rev0.1 99.2.1

Symbol	Parameter	Min	Max	(unit)
T_cyc	CLK Cycle Time	30	-	(ns)
T_high	CLK High Time	11	-	(ns)
T_low	CLK Low Time	11	-	(ns)

Symbol	Parameter	Min	Max	(unit)
T_su1	Bus input setup time to CLK	7	-	(ns)
T_su2	GNTN setup time to CLK	10	-	(ns)
T_h	Input hold time to CLK	0	-	(ns)

Figure 15.2.4.2 PCI Bus AC timing (output)



rev0.2 99.4.1

Symbol	Parameter	Min	Max	(unit)
T_val	CLK to OUT valid delay	2	11	(ns)
T_on	float to Active delay	2	-	(ns)
T_off	Active to Float delay	-	28	(ns)

Note: T_val(min) load is 10pF with 1kohm pullup and 1kohm pulldown
T_val (max) load for rise wave is 10pF with 25ohm pulldown
T_val (max) load for fall wave is 10pF with 25ohm pullup
Device test will be done with tester capacitive load.

15.2.5 Misc AC timing

AC caracteristics of SYSRSTN and TAKE_PICN

Figure 15.2.5.1 SYSRSTN,TAKE_PICN AC timing (input)

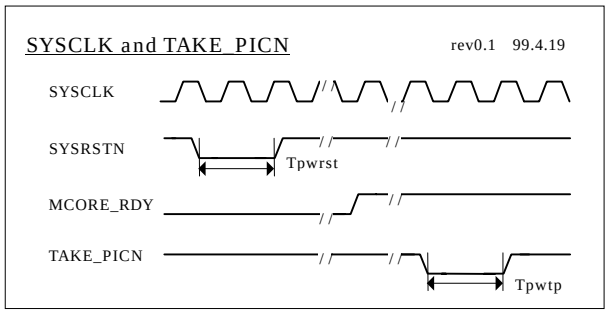


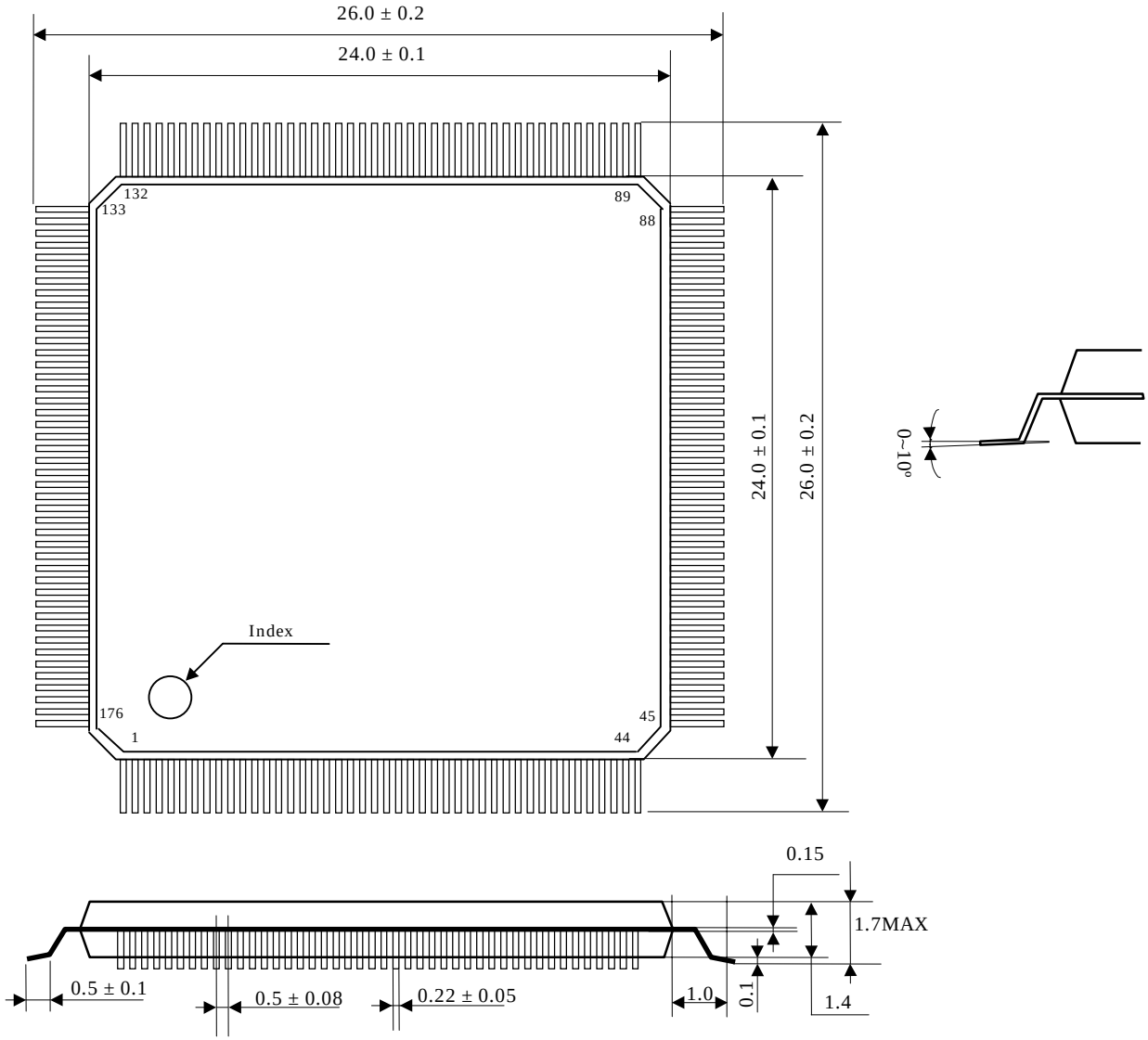
Table 15.2.5.1 SYSRSTN,TAKE_PICN AC timing (input)

No.	Symbol	Parameter	Min.	Typ.	Max.	unit	Note
1	Tpwrst	SYSRSTN assert pulse width	2	--	--	Tsys	Asynchronous signal more than 2T of SYSCLK
2	Tpwtp	TAKE_PICN assert pulse width	2	--	--	Tsys	Asynchronous signal more than 2T of SYSCLK

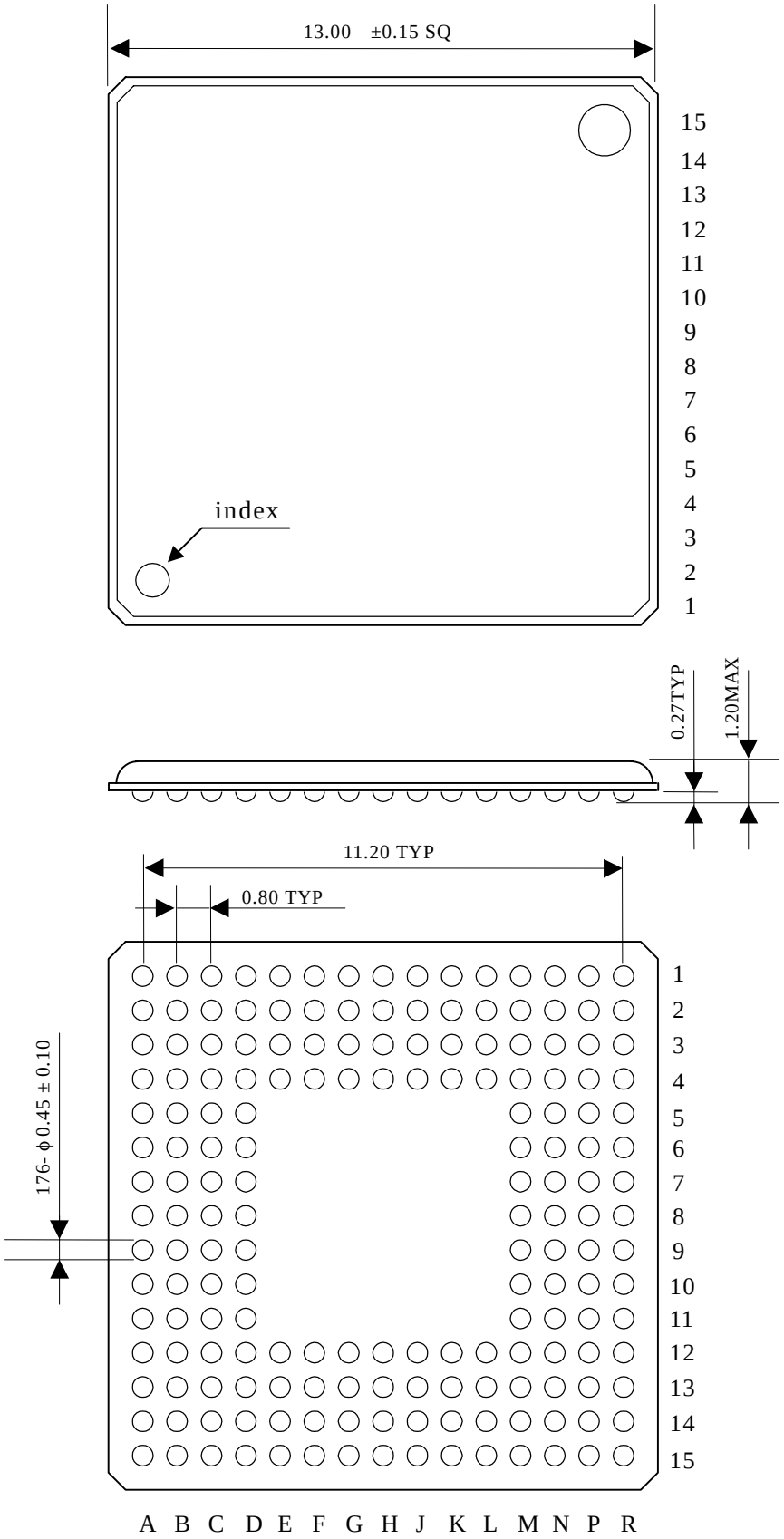
16. Package outline

The package outline of LQFP176 and TFBGA176 is shown below.

LQFP176 package outline



TFBGA176 package outline



17. known bug

BG#1. Incorrect operation at the multi-data transfer in PCI target mode

(Problem) When external PCI master accesses LSI, if it accesses by multi-data transfer (FRAMEN=L& IRDY=L), the right value will not be written in at the memory write, and the operation will not match the PCI specification at the config read/write.

(Solution) Target access to LSI is limited only as single data transfer (FRAMEN=H & IRDYN=L). Not to write/read with incrementing the address by software, application, driver and BIOS must be restricted about the operation.

BG#2 Bug about the Master Data Latency in PCI target mode

(Problem) When external PCI master reads LSI by single data transfer, if the time from FRAMEN=L to IRDNY=L of a master is more than 5T (specification a maximum of 8T), TRDYN will be asserted and negateed before IRDYN assert, this violated the handshake specification of PCI.

Moreover, about config read/write, normal operation can be guaranteed to MDL not more than 2T.

(Solution) Target access of LSI must be single data transfer and Master Data Latency (time from FRAMEN=L to IRDYN=L) must be a maximum of 2T.

BG#3 Parity error detect bug at PCI target and master mode

(Problem) The parity error of AD [31:0], CBEN [3:0], and PAR cannot be correctly detected and an applicable register cannot be updated at the time of data writing in PCI target mode and read-out in PCI master mode.

(Solution) Support of parity error detection is not performed as a video capture device.

BG#4 The processing of address parity error in the PCI target mode is not correct

(Problem) Even if an address parity error occurs in PCI target mode, specified processing is not performed but processing is continued.

Processing which should originally be taken when a device parity error response bit (config 04h [6]) is 1 :

1) Asserts SERRN, respose to the transaction and end as there was no error.

2) Assert SERRN, respose to the transaction and carry out target abort.

3) Assert SERRN, don't respose to the transaction and carry out target abort.

(Solution) Support of parity error detection is not performed and there is also no SERRN signal, it does not assert as a video capture device.

Response to an address parity error is taken as this.

BG#5 De-compressed picture data loss depending on the refreshment timing

(Problem) Last de-compressed picture data is transmitted to MCC from VRJ at the time of still picture de-compression, and if refreshment occurs immediately after asserting internal IRQ, processing will be ended, without writing de-compressed picture data for a maximum of 4 words to SDRAM.

(Solution) None

BG#6 At the time of a display, the end of a line does not become complete and flickers.

(Problem) Since synchronization of PCLK and SYSCLK has not done well the term which outputs picture data of the direction of a line at a display, there is a line which not match with H_COUNT.

(Solution) None

BG#7 De-compressed picture data may not be correctly outputted to SDRAM at the time of continuous de-compression.

(Problem) The de-compressed picture data outputted from VRJPEG lost inside MCC, and is not outputted to SDRAM occurs at random.

(Solution) None

This document is preliminary version and may be changed without notice.

Kawasaki Steel Corporation reserves the right to make changes to the specifications herein at any time without notice.

Kawasaki Steel Corporation does not assume any responsibility or liability arising out of the application or use of any circuit or information described herein; neither does it convey any license under its patent rights, intellectual property rights, or any other rights of Kawasaki Steel Corporation or of third parties.

Kawasaki Steel corporation
LSI division

1-3 B11, Nakase, Mihama-ku,
Chiba 261-8501, Japan
TEL +81 43(296)7412
FAX +81 43(296)7419